

3D FRACTURE MECHANICS ANALYSIS OF UNDERFILL DELAMINATION FOR FLIP CHIP PACKAGES

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ABSTRACT:

In flip-chip package, the mismatch of thermal expansion coefficients between the silicon die, copper heat spreader and packaging substrate induces concentrated stress field around the edges and corners of silicon die during assembly, testing and services. The concentrated stresses result in delamination on various interfaces involving a range of length scales from hundreds of nanometers to millimeters. Among these failures underfill delamination is a dominant failure mode. In this paper, a full parametric 3D model of flip chip package with heat spreader is developed with the capability of explicit modeling of 3D cracks. The crack driving force is computed as the functions of underfill properties including coefficient of thermal expansion and Young's modulus, as well as underfill fillet dimensions. The impact of different shapes of crack front is also investigated. The results show that underfill properties need to be optimized to minimize the occurrence of underfill delamination at the die corner. The results also show that there exists an optimal range of underfill fillet height to balance the manufacturability and reliability.

KEY WORDS: underfill, delamination, 3D, FEA

NOMENCLATURE

| | |
|-----|----------------------|
| E | Young's modulus, GPa |
| G | Energy release rate |
| a | crack size |

Greek symbols

| | |
|----------|--|
| α | Coefficient of thermal expansion (CTE) |
| ν | Poisson's ratio |

INTRODUCTION

It is well known that underfill has significant impact on flip chip package reliability. Organic substrate flip chip technology with underfill provides a cost effective solution to the demands of electronic packaging industry for increased reliability. Underfill protects solder bumps by considerably reducing the stress to the solder bumps. However, underfill itself is subject to shear or peeling stress and consequently, may induce additional failure modes. For instance, imperfect underfill with voids or microcracks will produce cracks or delamination under temperature cycling conditions.

Delamination at bimaterial interfaces such as underfill and die passivation or underfill and substrate solder mask, driven by coefficient of thermal expansion (CTE) mismatch between organic substrate and silicon die, is one of the dominant failure modes in presence of imperfect underfill. Once underfill delamination, occurs, the failure usually results in solder bump fatigue crack because of the loss of underfill protection and stress concentration arising from the underfill delamination.

In conventional stress analysis, a material is assumed to be free of defects. However, the junction of the three dimensional die corner and underfill is the potential failure site due to the presence of split singularity [1, 2]. The strength of singularity depends on the associated material properties and geometries. The delamination initiated from die edge takes a form of interfacial microcrack. In addition, initial delamination may also be the consequence of formation of microcracks or voids during dispensing process or surface contamination. Initial flaws are unavoidable in underfill. Hence preventing the flaw propagation as an unstable crack becomes important.

The purpose of this paper is to study the effects of various design variables including underfill modulus, CTE, fillet dimensions on the energy release rate (ERR) of underfill delamination by using 3D fracture mechanics analysis in ABAQUS.

MODEL

Since temperature cycling is the cause of the failures studied in this paper, thermal excursion from 125C to room temperature 25C is used as the temperature loading. The flip-chip is assumed to be in stress-free state at 125C, which is the typical glass transition temperature of epoxy underfill.

Most material properties are assumed to be isotropic linear elastic. Although high-Pb or eutectic solder is essentially rate and temperature dependent, material nonlinearity is not the focus of this work and will not be considered. Underfill material is assumed to behave linear elastically.

As shown in Fig. 1, a quarter model of a three dimensional flip-chip is built up in ABAQUS for finite element analysis (FEA). ABAQUS is a powerful modeling tool that provides great flexibility of parametric modeling. In this study, a

parametric flip chip model with capability of automatic crack generation was created. Geometrical model includes silicon die (20 mm wide, 0.8 mm thick), organic package substrate (40 mm wide, 1.4 mm thick), epoxy underfill (0.09 mm thick), copper lid, gel-like TIM between die and lid, and adhesive for lid bonding with package substrate. It is also noteworthy that in this study the fillet shape is sketched with curvature close to reality and also with the flexibility to model different fillet width and fillet height. Only a quarter of the flip chip package is modeled because of symmetric geometry and loading conditions. All materials properties are tabulated in Table 1. A pre-existing crack is inserted along the interface from die corner between silicon die and underfill with the crack front convex inwards, as illustrated in Fig. 2. The upper part is silicon die (die passivation is neglected in the model), and the lower part is underfill. In order to illustrate the crack profile, fillet and all other materials are intentionally not shown here. The crack replicates the situation where a micro-crack is initiated from the die edge or an existing flaw due to non-clean surface. Fig. 2 also explains the definition of crack size a in this 3D model.

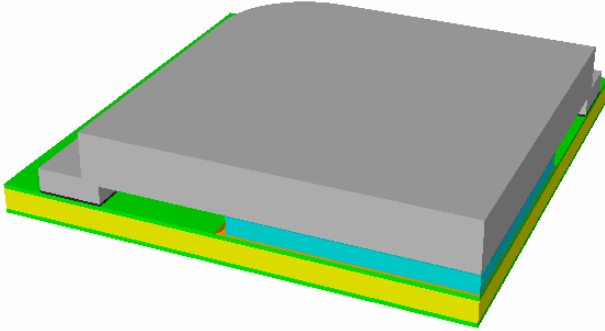


Figure 1. FEA model of a quarter symmetric package

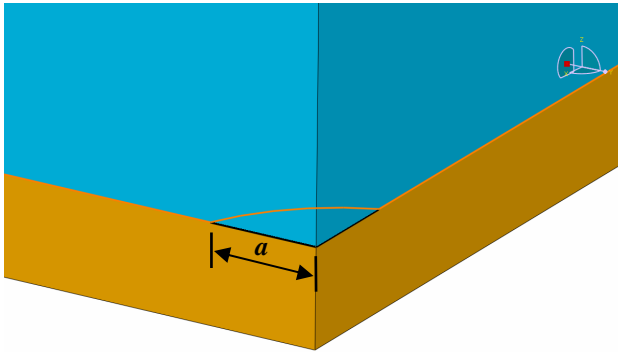


Fig. 2. Corner Crack Configuration

Table 1. Material properties for flip chip package

| Materials | E (GPa) | ν | α (ppm/C) |
|-----------------|-----------|-------|------------------|
| Silicon die | 130 | 0.28 | 3.3 |
| Underfill | 6 | 0.32 | 36 |
| Copper lid | 115 | 0.3 | 17.7 |
| Lid adhesive | 3.3e-3 | 0.3 | 300 |
| TIM | 6e-3 | 0.3 | 50 |
| Package buildup | 27.3 | 0.3 | 20 |
| Package core | 38 | 0.2 | 15.5 |

The design factors studied in this paper are:

- (1) Shape of crack front;
- (2) Underfill material properties (Young's modulus and CTE);
- (3) Underfill fillet height;
- (4) Crack size;
- (5) Comparison of results for lidded and lidless packages.
- (6) Comparison of results from 3D and 2D modeling.

In order to study the effect of underfill material properties, we vary the modulus from 3 to 9 GPa, CTE from 20 to 50 ppm/C. These variations allow full characterization of the individual as well as coupled effects of underfill mechanical properties on fracture parameters. Baseline case assumes elastic modulus = 6 GPa and CTE = 36 ppm/°C for the underfill, as listed in Table 1.

The influence of fillet height around die corner on underfill delamination is investigated by varying the baseline case, which assumes fillet of half coverage, i.e. the fillet height is half of die thickness, to the extreme configurations: no coverage and full coverage. These fillet configurations are intended to mimic properly encapsulated, under encapsulated and over encapsulated situations resulted from varied underfill dispense conditions.

Note that in the following presentation, the loading is temperature drop $\Delta T = 1^\circ\text{C}$. Therefore, from underfill glass transition temperature (125°C) to room temperature, the energy release rate (ERR) should be multiplied by a factor of 10^4 .

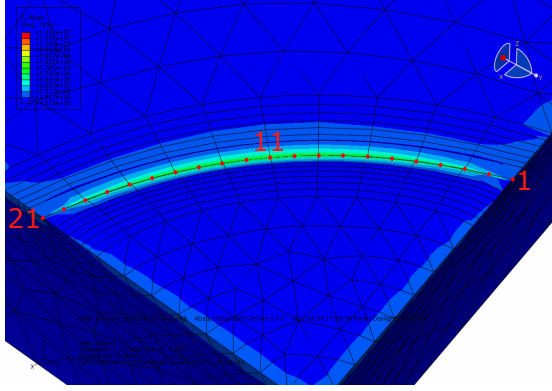
RESULTS AND DISCUSSIONS

Distribution of ERR along crack front

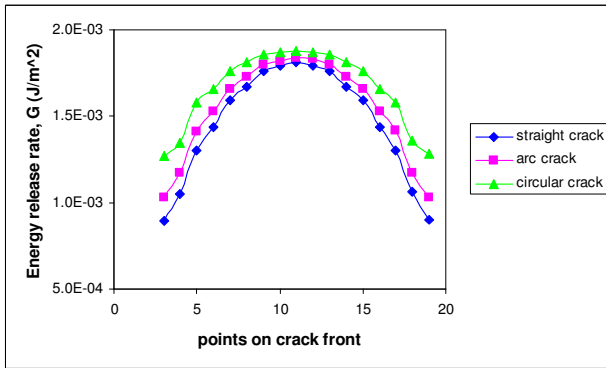
Since in this study, a full 3D fracture mechanics-based FEA model is developed with explicit modeling capability of 3D crack. Along the whole crack front, the energy release rate (ERR) has a spatial distribution. The position with maximum ERR will propagate firstly. Therefore, the shape of the crack front will converge to a shape in favor of the fastest energy release. In this Fig. 3, we present the results for three different crack front profile, straight crack, arc crack and circular crack. The so called "straight crack" means the crack front is a straight line from point 1 to point 21; the "arc crack" means the crack front bows inwards to some extent; while the "circular crack" means that the crack front is a part of circle, just as penny crack; see Fig. 3(a). For all three cases, the ERR has the similar distribution with slight shift upwards if the

crack front moves inwards, as shown in Fig. 3(b). So the mid point 11 always has the maximum ERR, which means the crack prefers to propagate inwards from the center of the crack front.

If the die is rectangular instead of square, the distribution profile skews to a little extent.



(a)



(b)

Fig. 3. (a) Stress field at the crack front (b) energy release rate vs. crack front location

Effect of underfill modulus

Fig. 4 plots the energy release rate, G , as a function of underfill modulus, E , for different CTE with fixed crack size $a=10\mu\text{m}$. The G either increases or decreases with the increase of modulus E , depending on CTE and crack size. For high CTE (40ppm/C) and small cracks ($<20\mu\text{m}$), G increases with E ; otherwise G decreases with E . For CTE in the range of 30-40ppm/C, G is insensitive to E .

The trends of either up or down in Fig. 4 are not captured by previous studies. The complex trends vs. underfill modulus underlines the facts that the ERR dependence on underfill modulus is not straightforward: it also depends on other factors including underfill CTE, crack size, die size, die aspect

ratio, fillet profile, etc, and the interactions among these factors. The choice of underfill modulus needs to take into consideration of the other factors to mitigate the risk of underfill delamination.

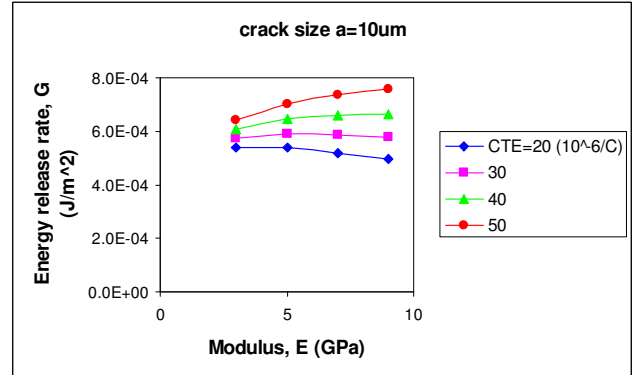


Fig. 4. Energy release rate is plotted as a function of underfill modulus for different CTE with fixed crack size $a=10\mu\text{m}$. The G either increases or decreases with the increase of modulus E , depending on CTE and crack size.

Effect of underfill CTE

Fig. 5 plots the energy release rate, G , as a function of underfill CTE, i.e. α , for different CTE with fixed crack size $a=100\mu\text{m}$. In general the higher ERR will be produced by the higher CTE, despite the sensitivity is moderate. For instance, energy release rate increases by nearly 30% if underfill CTE varies from 20 ppm/C to 50 ppm/C.

The effect of underfill CTE on ERR, as shown in Figure 5, clearly demonstrates that, in addition to global CTE mismatch between silicon die, copper lid and organic substrate, the local CTE mismatch among die and underfill also play a viable role in determining fracture behavior for underfill delamination. The results validate the general recommendation of lower-CTE underfill.

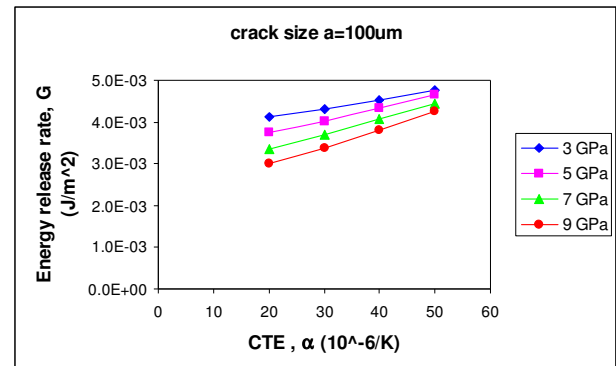


Fig. 5. Energy release rate is plotted as a function of underfill CTE for different modulus with fixed crack size $a=100\mu\text{m}$.

Effect of crack size

Fig. 6 plots the energy release rate as a function of crack size for different modulus with fixed CTE=20ppm/C. The G increases rapidly with the propagation of crack in all the cases. Once the crack is initiated, it will continue to grow.

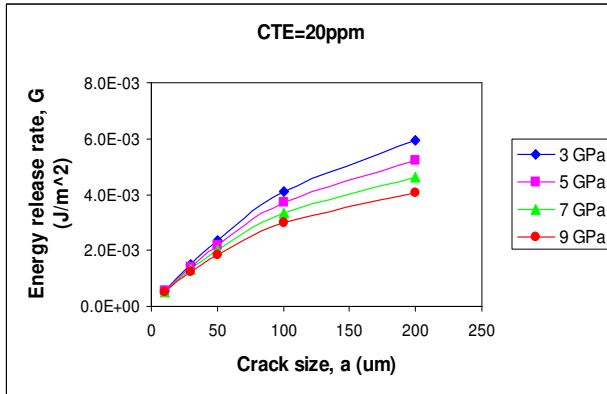


Fig. 6. Energy release rate is plotted as a function of crack size for different modulus with fixed CTE=20ppm/C.

Effect of underfill fillet height

Fig. 7 plots the energy release rate as a function of normalized fillet height for baseline case. The energy release rate for different temperature excursions can be readily obtained from the fact that energy release rate is proportional to $(\Delta T)^2$. As shown in Fig. 7, the energy release rate G decreases with increasing fillet height. Therefore, the taller underfill fillet is critical to reducing the risk of underfill delamination.

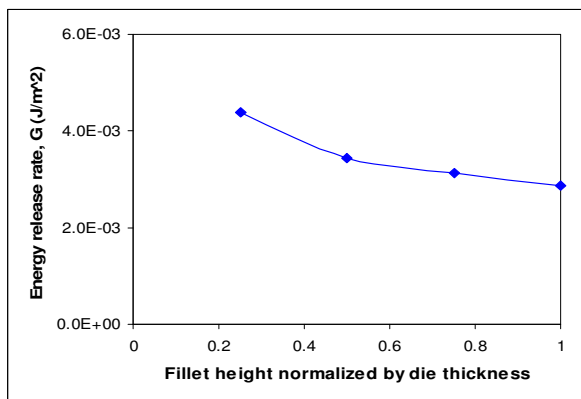


Fig. 7. Effect of fillet height on energy release rate.

Comparison of lidded and lidless packages

Fig. 8 plots the energy release rate as a function of underfill modulus for two different packages: lidded and lidless. Same trends are exhibited for either lidded or lidless packages, despite in different magnitudes. The lidded package, however,

produces approximately 2~3 times higher ERR than in the lidless package.

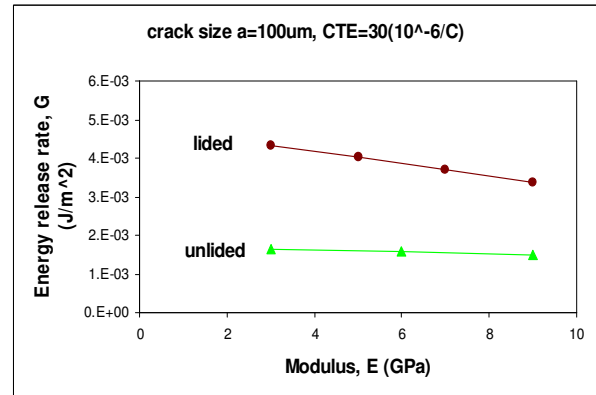
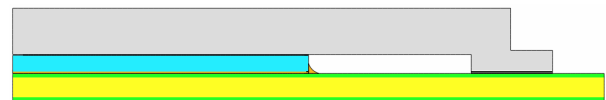


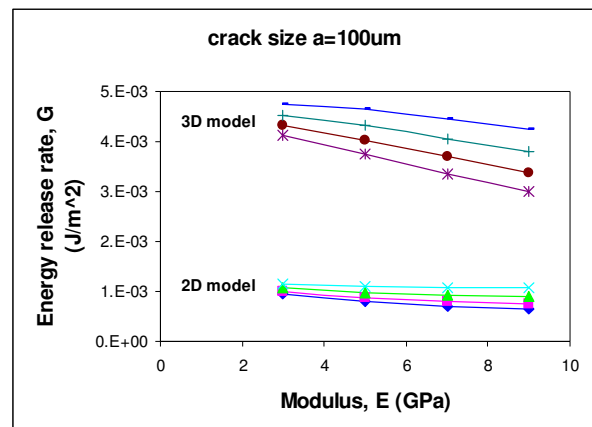
Fig. 8. Comparison of lidded and lidless packages.

Comparison of 3D model and 2D model

Fig. 9 plots the G as a function of E for both 3D model and 2D plane strain models. Both 3D and 2D models show the same characteristics. However, 3D crack, in the same crack length, produces 3~5 times greater crack driving force than in the 2D crack. 2D model does predict correct trend, except significantly underestimating the magnitude of crack driving force.



(a)



(b)

Fig. 9. (a) A half model to 2D flip chip in FEA. (b) Comparison of 3D model and 2D model.

CONCLUSIONS

It has been demonstrated that it is possible to optimize design factors to reduce the risk of underfill delamination. The design factors studied in this paper involve material properties including elastic modulus and CTE, underfill fillet height, crack size, thermal solution, i.e. lidded and lidless through both 3D model and 2D model. From the results we find that underfill delamination for this particular flip chip configuration exhibits instability as the energy release rate increases with crack length. We found that the crack driving force is in general insensitive to the underfill modulus in the range between 3 and 9 GPa. Furthermore, the dependence on underfill modulus is affected by the interaction with other factors such as underfill CTE, etc. It is evident that lower-CTE underfill is always favorable to reduce the energy release rate. Increasing fillet height is proved to be effective to prevent underfill delamination. Lower fillet (under encapsulation) has the highest probability of causing underfill delamination because it results in higher energy release rate. The lidded package has about 2~3 times larger G than lidless package. 2D model predicts correct trend, but results need to scale up 3~5 times to reflect 3D nature.

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