Stress in Flip-Chip Solder Bumps due to Package Warpage -- Matt Pharr

Introduction

As the size of microelectronic devices continues to decrease, interconnects in the devices are scaling down correspondingly. Meanwhile, the demand for performance in terms of current capacity continues to increase. The coupling of these two trends leads to a drastically increasing current density in the devices during operation. One of the most significant problems associated with this large current density is a process known as electromigration that is observed in the solder bumps that connect the integrated circuit chips to external circuitry (see Figure 1).

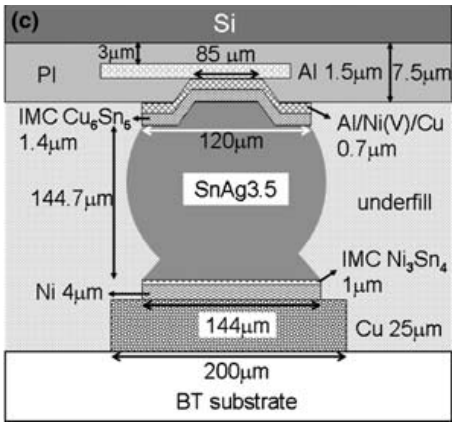

Figure 1: Layout of typical flip chip solder bump joining interconnect line to conducting trace [1].

Electromigration is mass transport due to atomic displacement resulting from an electric field. As electrons move through a metal lattice, they tend to scatter at imperfections or by interactions due to phonon vibrations. This scattering results in change in the momentum of the electrons and hence exerts a force on the metal ions known as the wind force and given by $F_{wind} = Z^* e \rho j$, where Z^* is the effective charge number, e is the charge of the electron, ρ is the resistivity, and j is the current density [2]. Hence, one can see that this force is directly proportional to the current density, and above some threshold, this force is large enough to motivate atoms to diffuse from their original positions in the direction of the electron flow. The threshold current density is much smaller in the solder bump than in the Al and Cu interconnects that the solder joins; thus, electromigration in the solder bump can be significant. Furthermore, it has been suggested that the diffusion of atoms caused by electromigration creates tension upstream and compression downstream [3]. Experimental evidence verifies this idea as voids (created under tensile stress) are seen upstream in the solder bumps (see Figure 2). Accumulation and propagation of these voids leads to increased electrical resistance and eventual failure of the solder bump. However, electromigration is only one factor in the creation of the voids; a wide range of others including chemical potential, temperature, creep, and mechanical stress may play additional roles.

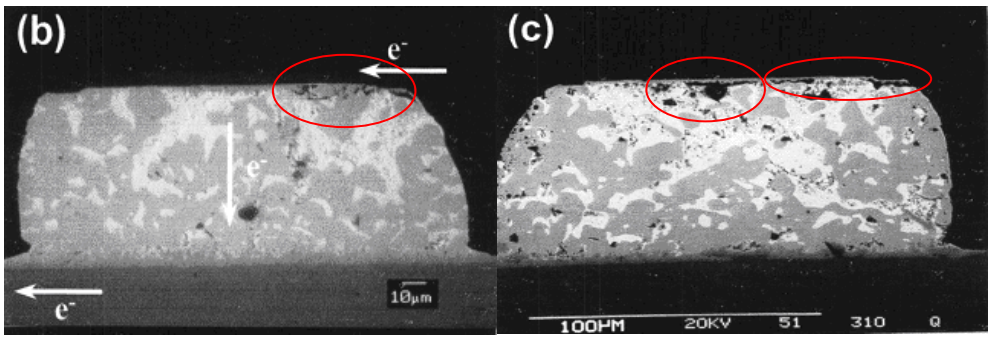

Figure 2: Formation of Voids due Electromigration in a Flip Chip Solder Joint. The voids have been circled and they are clearly upstream in the electron flow [4].

Dr. Zhigang Suo has proposed a model that couples creep and self-diffusion (in the case of the solder the wind force drives the self-diffusion) [5]. He and I currently are attempting to apply this theory to the solder bump during operation. One factor that we want to take into consideration is a residual mechanical stress, as it has been observed experimentally that an applied mechanical stress decreases the mean time to failure of the solder bump (see Figure 3). Such a stress is introduced naturally during operation due to the thermal mismatch between the Si die on one side of the solder bump and the substrate (a printed circuit board – PCB) on the other (Figure 1). To permanently connect the solder to the rest of the system, the solder is heated up to its melting point to produce an electrical connection and is subsequently cooled to room temperature. The temperature of the system is then increased again during operation of the device [6]. This results in warpage (increased curvature) of the substrate during operation, which can lead to various mechanical stresses being placed on the solder bumps. Accurate estimation of these naturally occurring mechanical stresses will allow us to predict how much of a role they have in the overall stress state of the solder bump compared to the other factors such as creep coupled with electromigration.

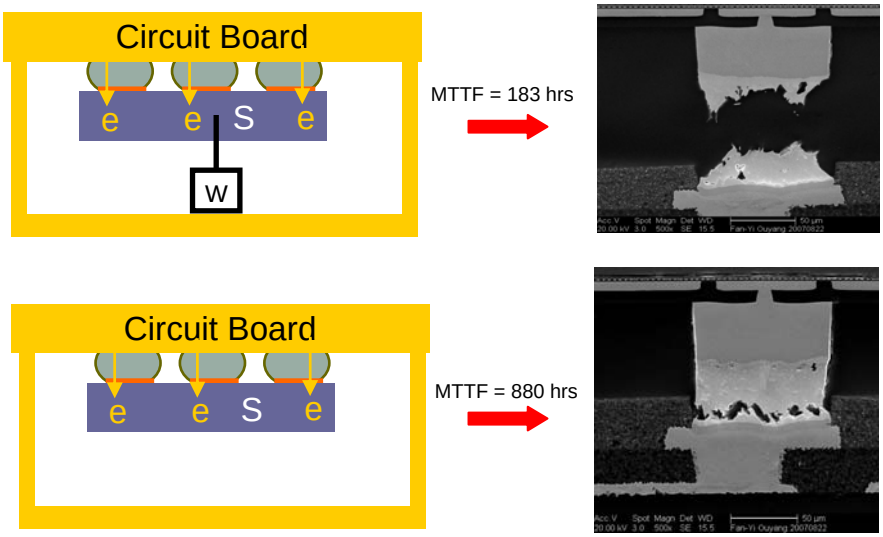

Figure 3: Experiments indicate that when an external mechanical load is applied to the flip-chip, the mean-time-to-failure is drastically reduced.

Finite Element Model Description

Finite element analysis was employed to predict mechanical stress levels in these solder bumps due to temperature change during assembly and operation. The model took into account the Si die, the PCB substrate, the solder bumps, and the underfill, with the geometry and mechanical properties given in Figures 4 and Table 1, respectively.

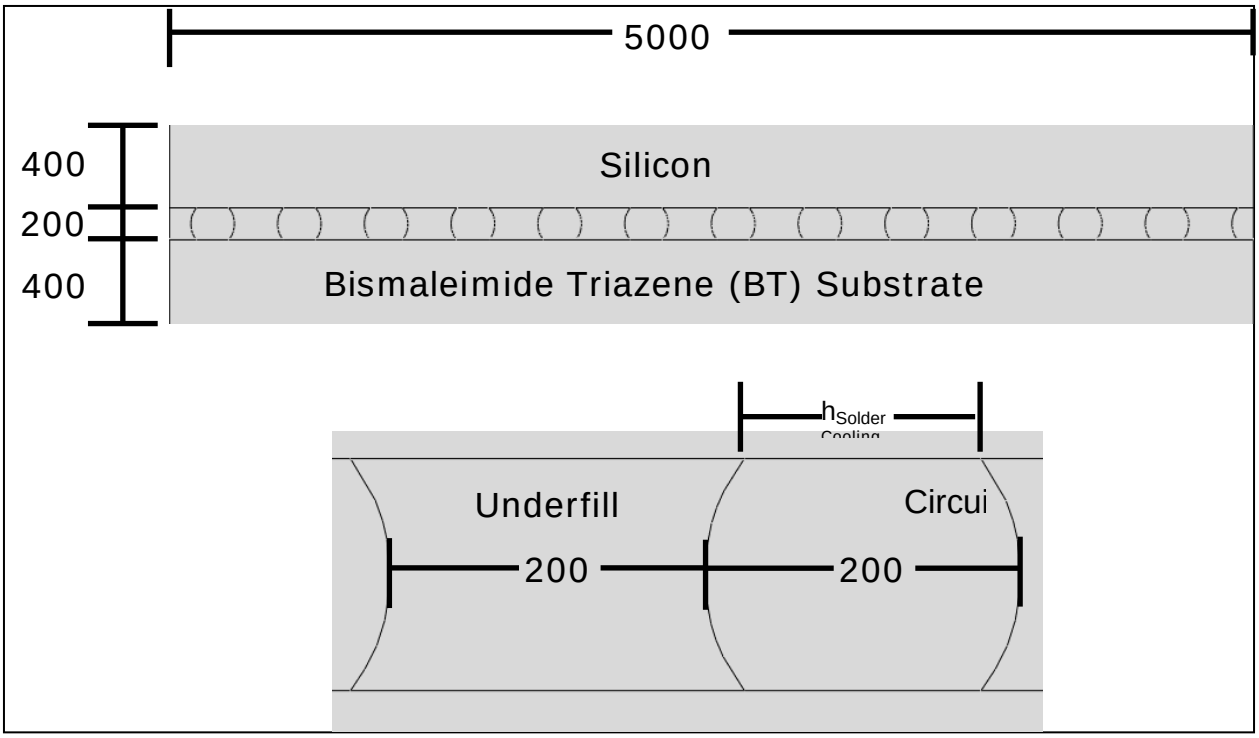

Figure 4: Geometry used in simulation. All dimensions are in μm. It was assumed the chip is symmetric about its right edge.

Material	Young's Modulus, E (GPa)	Poisson's Ratio (ν)	Thermal Exp. Coefficient (10-6/K)
Sn-3.5Ag Solder	50	0.3	23
Underfill	6	0.35	30
Silicon chip	131	0.3	2.8
Bismaleimide Triazene (BT) Substrate	26	0.39	15

Table 1: Materials properties of components [7]

The system was approximated as a 2D system and a mesh was created with 4-node linear coupled temperature-displacement quadrilateral elements. As one can see in Figure 6, the mesh is fairly fine, as it is the author's opinion that one might as well create a fine mesh to improve accuracy as long as it does not take too long to run. (In this case, the simulations usually took about 2 minutes.) Furthermore, the mesh is refined near regions of interest such as the solder bumps and the edges.

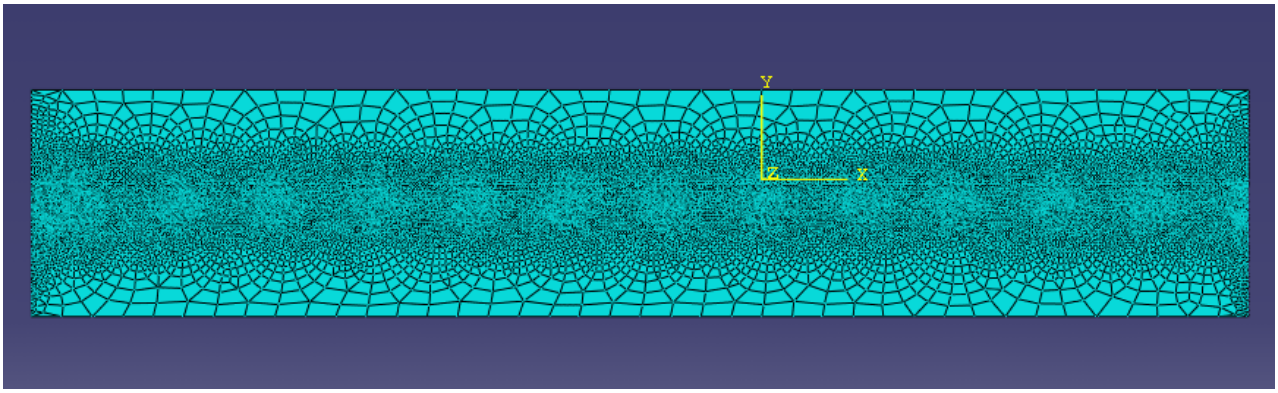

Figure 5: System mesh

Then, the study was performed following the outline below:

- *Step 1: 221°C – melting point of solder*
- *Step 2: 23°C*
  - *Coupled temp-disp steady state*
  - *x-Symmetry Condition on Right End*
- *Step 3 (Attempted): 1A current through solder*
  - *Coupled thermal-electric*
  - *Inputted thermal properties of materials*
  - *Did not converge*
- *Step 3: (Actually Used) Solder and underfill at 100°C; linear variation in substrate and Si to ambient temp of 70°C*
  - *Used subroutine to define this temperature field*

It was assumed that the solder fully demonstrated properties of a solid directly below its melting point. This assumption is not completely correct as it really still exhibits some liquid-like behavior at elevated temperatures, but modeling of such behavior is extremely advanced, and the author's knowledge of finite elements is too elementary as to perform such a study. Also, it should be noted that the original goal was to implement the coupled thermal-electric routine built into Abaqus in addition to the coupled temperature-displacement routine to more fully capture the thermal, mechanical, and electrical interactions that are present in this complicated system. The thermal and electric coupling comes about through Joule heating that occurs when a current is passed through a conductor. The basic idea is that moving electrons that form the current impart some of their kinetic energy to the ions of the conductor, increasing the conductor's temperature. In the Abaqus model, natural convection was allowed for at the free-surfaces of the material and all of the pertinent thermal properties were assigned to each material. However, as is noted in the outline, this part of the study would not converge. Fortunately, this problem was circumvented by finding some experimental data for flip-chips that indicated that the solders heat up to approximately 100°C during operation and that the free surfaces are approximately 70°C [1]. So, a linear variation between these known data points was assumed and was implemented using a subroutine to define the temperature field. The results of the study after all the aforementioned steps are performed are given in the following section.

Results

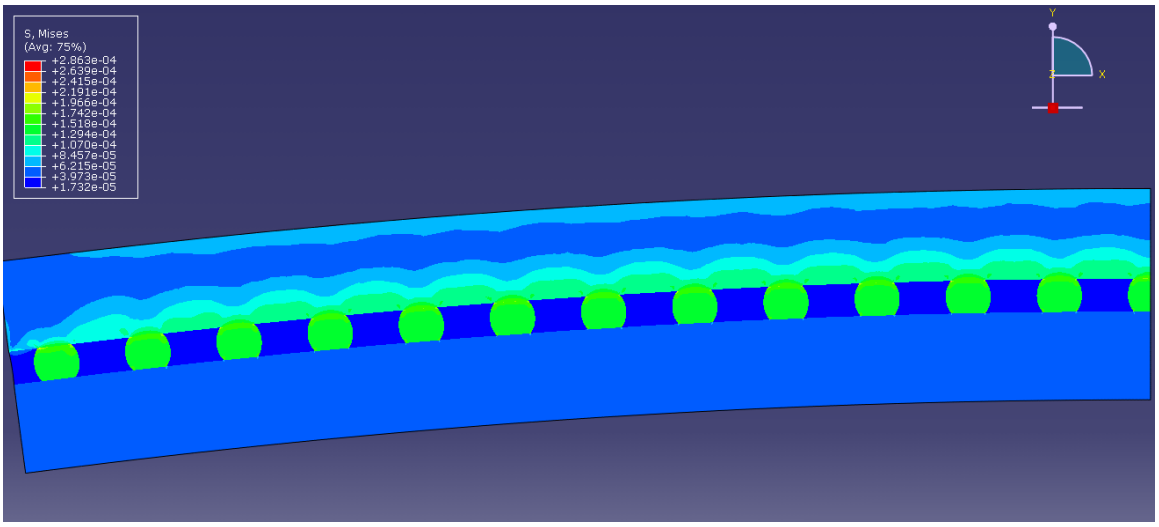

Figure 6: Mises Stress

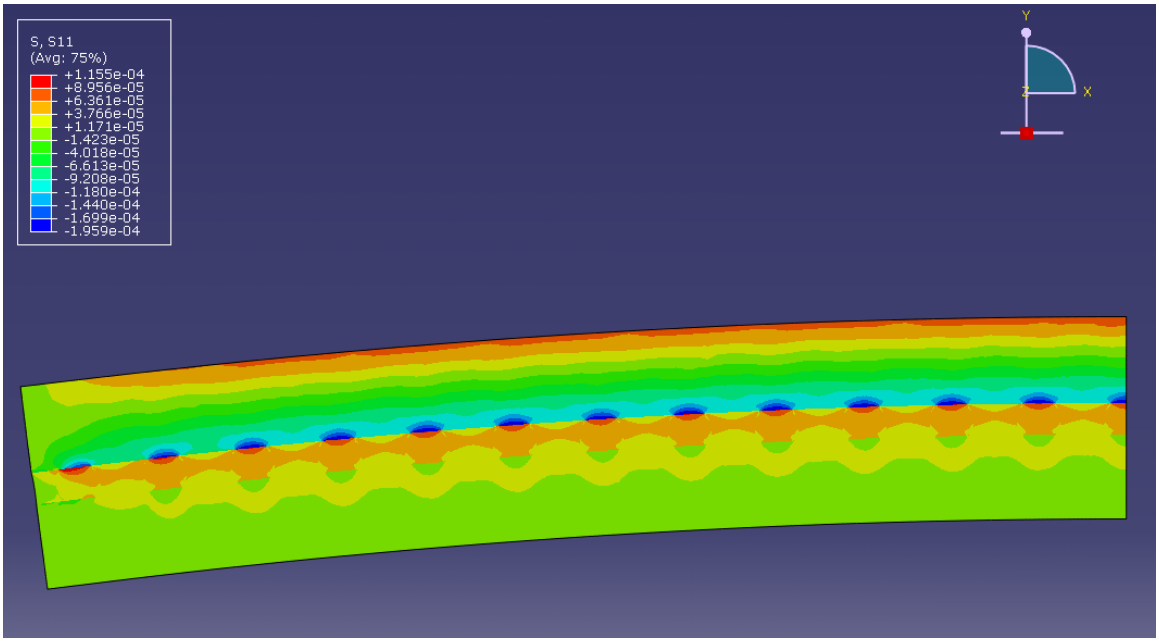

Figure 7: σ_{11}

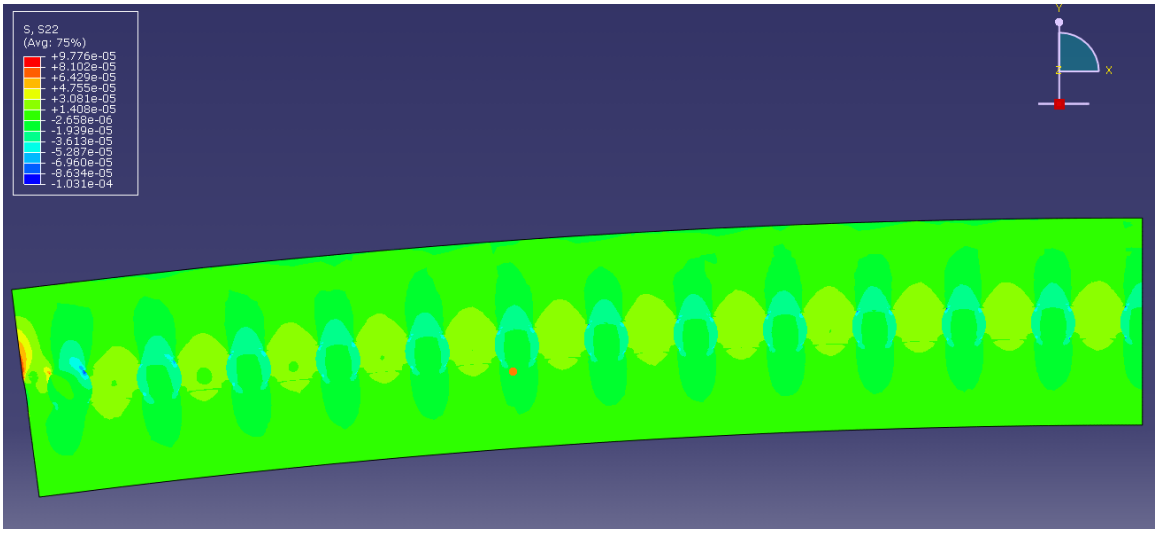

Figure 8: σ_{22}

From Figures 6-8, one can make some interesting observations. In Figure 6, the Mises stress in the solder bumps was found to be about 150 MPa, with little variation among the solder bumps and within each bump. Figure 7 demonstrates that the maximum σ_{11} stress of a bump near the left side of the figure was about 108 MPa, and the σ_{11} stress in a bump near the right side of the figure was about 90 MPa. Also, one can see that there is a large variation in stress within each solder bump. Finally, the stress component that is of most interest to the author (to compare a theoretical model to an observed system) is σ_{22}. It is observed in the study that the stress was about 20 MPa in the bumps and had only a slight variation within each bump and among all the bumps. So, the most important result for the purposes of this study is that the stress, σ_{22}, in the solder bumps was found to be approximately 20 MPa in all the bumps.

Model Validation

Since there are no good experimental results available for this system and the geometry and multiple materials present in the model make this fairly difficult to solve analytically, it is hard to fully validate the results. However, one can make a few observations. First of all, the curvature of the system agrees with intuition. The solder starts in an essentially stress-free molten state. Above the solder bumps is the Si semiconductor, which is fairly stiff and has a relatively small coefficient of thermal expansion, and below the solder bumps is the circuit board, which is fairly compliant and has a relatively large coefficient of thermal expansion (Figure 9). It is assumed that the solder bumps solidify just below their melting point. At this point, the solder bumps become rigidly connected to the Si semiconductor and the circuit board. To get an idea of curvature, imagine that the Si is much stiffer than the circuit board so that it has no curvature upon cooling to room temperature (obviously this is not entirely correct but Si is much stiffer than the circuit board – see Figure 9). Since the circuit board has a fairly large coefficient of thermal expansion, it will try to shrink significantly upon cooling. However, the solder bumps will resist this shrinking since they are now rigidly connected to the circuit board. Still, the bottom surface of the circuit board will be essentially free to shrink and hence will contract more than the top surface. This situation will create a concave downward curvature (see Figure 9).

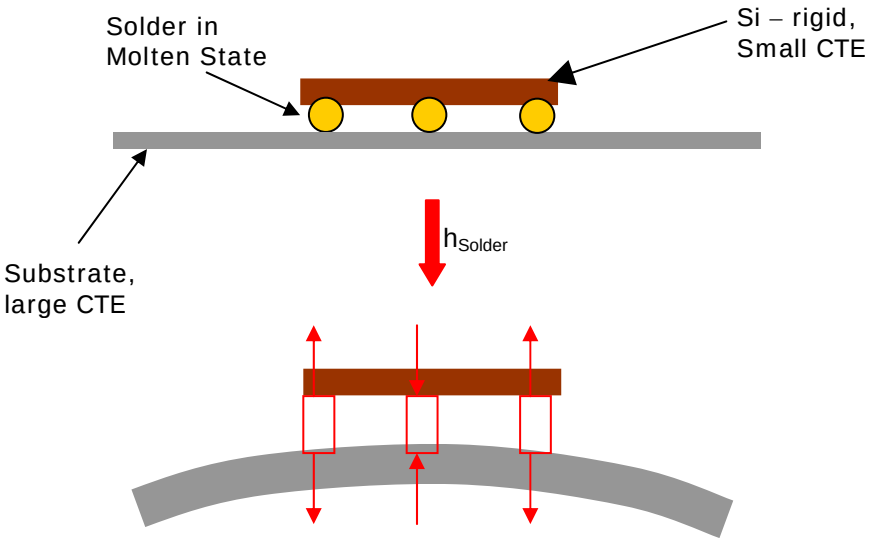

Figure 9: Predicted Curvature

This curvature is the same as is seen in Figures 6-8 so at least the Abaqus results agree qualitatively with the above physical intuition.

Another piece of evidence suggesting that these results seem at least reasonable is that Intel has told the author that they predict the σ_{22} stress in the solder due to this package warpage effect (from rough curvature measurement experiments) to be between 0 and 50 MPa, which was observed in the study.

Although it is difficult to develop an analytical model for the system model in Figures 6-8, one can easily develop an analytical solution for a thin layer of a material sandwiched between layers of another material that is cooled from an elevated temperature. A free body diagram of this scenario is depicted in Figure 10.

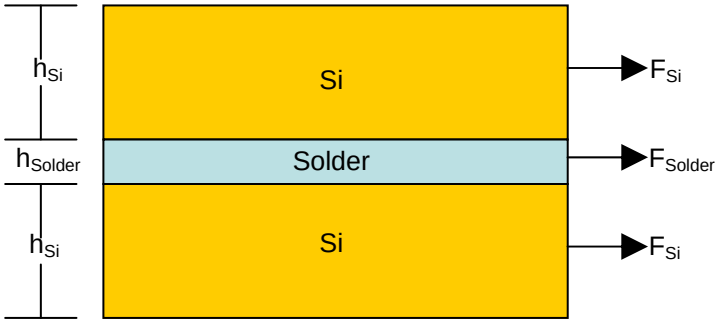

Figure 10: Free body diagram of one material sandwiched between two others

Away from the end of the materials, one expects the stress to be uniform in each material in the x-direction (this is essentially a 1D problem) since by Saint-Venant's principle one expects this end effect to be localized. With this approximation, one can easily calculate the stress in the solder away from its end as follows:

Deformation Geometry (since solder and silicon are bonded):

$$\varepsilon_{Si} = \varepsilon_{Solder}$$

Force balance:

$$2F_{Si} + F_{Solder} = 0$$
$$\Rightarrow 2\sigma_{Si}h_{Si} + \sigma_{Solder}h_{Solder} = 0$$

Material Model:

$$\varepsilon_{Si} = \frac{\sigma_{Si}}{E_{si}} - \nu_{Si}\frac{\sigma_{Si}}{E_{Si}} + \alpha_{Si}\left(T_{low} - T_{high}\right)$$
$$\varepsilon_{Solder} = \frac{\sigma_{Solder}}{E_{Solder}} - \nu_{Solder}\frac{\sigma_{Solder}}{E_{Solder}} + \alpha_{Solder}\left(T_{low} - T_{high}\right)$$

This is a system of 4 unknowns and 4 equations. The solution is:

$$\sigma_{Solder} = \frac{\left(\alpha_{Solder} - \alpha_{Si}\right)\left(T_{high} - T_{low}\right)}{\frac{1-\nu_{Solder}}{E_{Solder}} + \frac{1-\nu_{Si}}{E_{Si}}\left(\frac{h_{Solder}}{2h_{Si}}\right)}$$

Substituting in the relevant parameters from Table 1 and Figure 10, one obtains:

$$\sigma_{Solder} \approx 266.6MPa$$

The results of an Abaqus study on the system in Figure 10 are given on the next page.

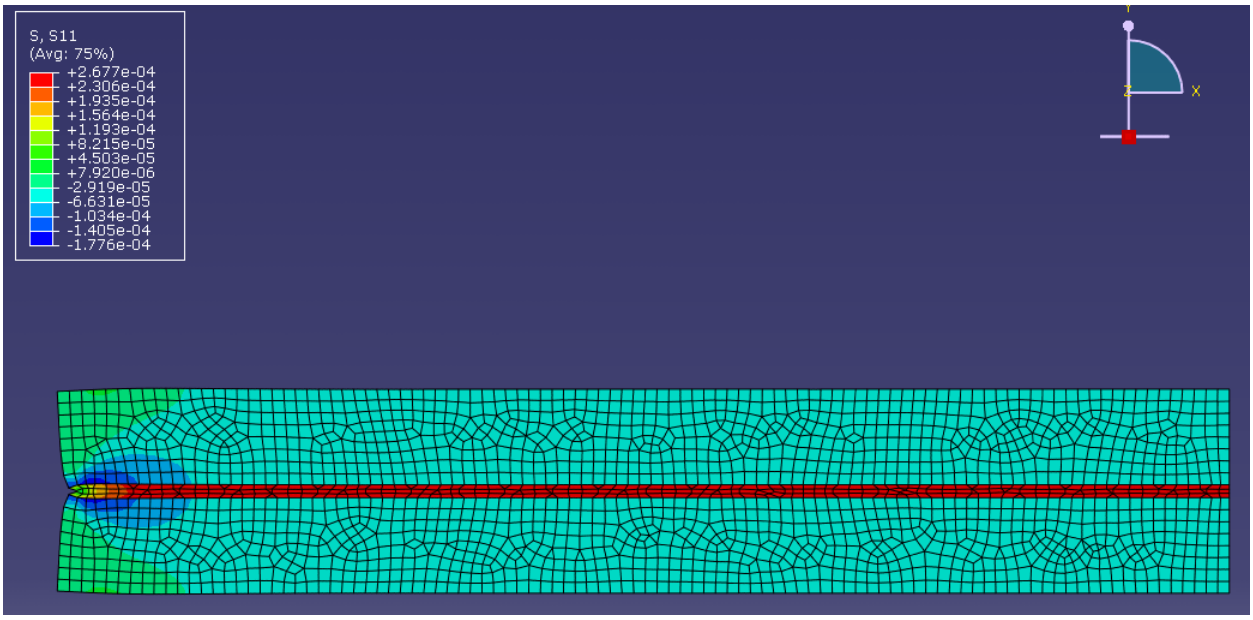

Figure 11: σ_{11} for system in Figure 10

From Figure 11, one can see that the stress in the solder layer (the red band in the figure) is about

$$\sigma_{Solder} \approx 2.667 * 10^{-4} \frac{N}{\mu m^2} = 266.7 MPa$$

The agreement with the previously developed analytical solution is excellent! Hence, it seems that Abaqus is highly capable of handling this class of thermal problems with various materials, which adds a great amount of validation to the results produced for the study discussed in the Results section.

Conclusions

The effect of temperature change during assembly and operation on the stress state of solder bumps in flip chips was examined using finite element analysis. The model took into account the Si die, the PCB substrate, the solder bumps, and the underfill. The stress state during operation was fully characterized; most notably, a stress of σ_{22} = 20 MPa was found. It was shown that the stress results seem fairly reasonable and that Abaqus is capable of producing results that are in agreement with analytical solutions for this general class of problems.

References

[1] C. Chen and S. W. Liang, 2007, "Electromigration issues in lead-free solder joints," J. Mater. Sci., **18**, pp. 259-268.

[2] K. N. Tu, 2003, "Recent advances on electromigration in very-large-scale-integration of interconnects," J. Appl. Phys., **94**, pp. 5451-5473.

[3] I.A. Blech and C. Herring, 1976, "Stress Generation by Electromigration," Appl. Phys. Lett., **29** pp. 131-133.

[4] E. C. C. Yeh, W. J. Choi, and K. N. Tu, P. Elenius, and H. Balkan, 2002, Appl. Phys. Lett., **80**, 580.

[5] Z. Suo, 2004, "A continuum theory that couples creep and self-diffusion," Journal of Applied Mechanics **71**, pp. 646-651.

[6] Tu, K.N. et al, "Physics and materials challenges for lead-free solders," J. Appl. Phy., Vol. 93, No. 3 (2003). 24, NO. 4 (2001), pp. 667- 672.

[7] Siewert, T.; Liu, S.; Smith, D. R.; and Madeni, J. C., (2002), "Database for Solder Properties with Emphasis on New Leadfree Solders," NIST & Colorado School of Mines, Release 4.0, Feb. 2002, available at http://www.boulder.nist.gov/div853/lead_free/solders.html