

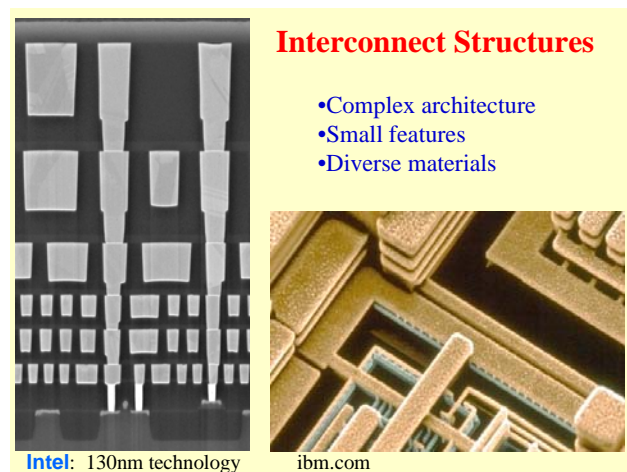
Lecture 11 Stress-Induced Voiding in Interconnects

This lecture is an abbreviated version of two sections in the following article. A PDF file of the article is available online www.deas.harvard.edu/suo, Publication 139.

Z. Suo, Reliability of interconnect structures. pp. 265-324 in Volume 8: *Interfacial and Nanoscale Failure* (W. Gerberich, W. Yang, Editors), *Comprehensive Structural Integrity* (I. Milne, R.O. Ritchie, B. Karimhaloo, Editors-in-Chief), Elsevier, Amsterdam, 2003.

On 23 January 1959, Robert Noyce wrote in his lab notebook: "... it would be desirable to make multiple devices on a single piece of silicon, in order to be able to make interconnections between devices as part of the manufacturing process, and thus reduce size, weight, etc. as well as cost per active device." With these words, the co-inventor (with Jack Kilby) of the integrated circuit, and the co-founder (with Gordon Moore) of Intel Corporation a decade later, spelled out the Monolithic Idea that would shape the microelectronic revolution (Reid, 1984). To function, transistors, capacitors, and resistors must connect among themselves and to the external world. Rather than first making these components individually and then connecting them with wires, the microelectronic technology fabricates the interconnect structure, as well as all the components, into a single solid piece, the *chip*.

Ever since, the technology has advanced by miniaturization, squeezing more and more transistors on every single chip. By necessity the interconnect structure has *complex architectures*, *diverse materials*, and *small feature sizes*. The figure shows a



transmission electron microscope image of an interconnect structure. The structure is a three-dimensional network of conductor lines embedded in a dielectric matrix, fabricated on the silicon surface that contains the active devices. The conductor lines are on several levels, and linked by vias. The lines have rectangular cross-sections and, on a given level, have a constant thickness but variable widths. A silicon nitride film caps the interconnect structure, serving as a barrier of the environmental molecules. Lithographically defined feature sizes, such as line width and via size, are as small as 100 nm. Films as thin as a few nanometers are used.

Traditional interconnect structures use aluminum as the conductor, and silica as the dielectric. Tungsten vias link the lines between the levels, and titanium nitride thin layers lie between the aluminum lines and the dielectric. To make faster devices, the conductor must have higher conductivity, and the dielectric must have lower dielectric constant. Copper has been used as the conductor lines in more recent interconnect structures (Rosenberg et al., 2000). The conductor lines at different levels are linked with copper vias. Liners such as tantalum lie between the conductor and the dielectric to prevent copper diffusion into the dielectric and to promote adhesion. Low dielectric constant materials of current use include an organic material known as SiLK (Martin et al., 2000), and a carbon doped oxide. The former is ductile, and the latter is brittle. Both are compliant compared to silicon dioxide. To further reduce the dielectric constant, other materials, including porous materials, will be used in future interconnects (Morgen et al., 1999).

The Monolithic Idea solves one problem, but creates another. Making reliable interconnect structures has been a persistent challenge. Stress results from material deposition, thermal expansion mismatch, and electromigration. Material deposition inevitably generates stress; for example, deposition of refractory metals such as tungsten usually generates stress of

GPa range. Materials in interconnect structures, selected to function as conductors, dielectrics, or barriers, have dissimilar thermal expansion coefficients. On cooling from the fabrication temperature, the structures acquire stresses. To fit into the small space, each conductor line must have a small cross-sectional area. The intense electric current motivates metal atoms to diffuse in the line, generating tension where atoms deplete, and compression where atoms accumulate.

The study of interconnect reliability has a long history. Electromigration has been a persistent concern ever since integrated circuits were mass-produced (Blech and Meieran, 1967). As atoms diffuse, voids grow and sever metal lines. Stress-induced voiding was observed in 1980s, when the technology brought the line width comparable to the line thickness (Curry et al., 1984). Such an aluminum line, of approximately square cross-section, encapsulated in silica, develops triaxial stresses of magnitude much above the yield strength of aluminum (Jones and Basehore, 1987). Voids grow to relax the stresses, facilitated by atomic diffusion (Sauter and Nix, 1992; Korhonen et al. 1993). Around the same time, thin film fracture mechanics was advanced (Evans et al., 1988; Hutchinson and Suo, 1991; Thouless, 1991), providing tools to quantify toughness of thin films (Ma et al., 1998; Cook and Liniger, 1999), and adhesion between thin films (Dauskardt et al., 1998). The tools have been incorporated into industrial practice in material selection, process control, and failure analysis.

More recently, a new failure mechanism has been identified, in which cracks grow in brittle films under cyclic temperatures, aided by ratcheting deformation in a metal underlayer (Huang et al., 2000). Stress-induced voiding has been observed in blanket copper films (Shaw et al. 2001, Sekiguchi et al., 2001), and in copper vias in the copper/silica interconnect structure (Hommel et al., 2001; Ogawa et al., 2002). Low dielectric constant materials invariably have

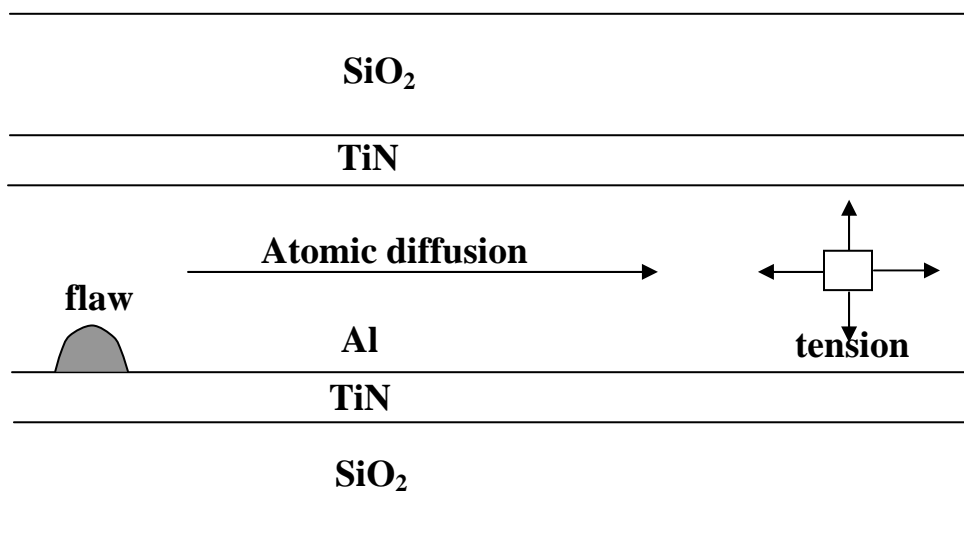
low stiffness; their effects on interconnect reliability are the focus of current studies (Lee et al., 2002; Ambrico et al., 2002; Liang et al., 2002; Rim et al., 2002).

This chapter is organized according to the failure modes in the interconnect structure: cracking, debonding, ratcheting, voiding, and electromigration. Such perversities are not only nuisances—problems to be tested away by trial-and-error, but also opportunities for fundamental study of the mechanical behavior of diverse materials, in integrated structures, at an unprecedented small size scale. The study of electromigration has led to the discovery that adding a few percent of copper into aluminum interconnects slows aluminum diffusion rate by nearly two orders of magnitude. The atomistic origin of this behavior is still not fully understood today. The observation of stress-induced voiding, perhaps more than any other single event, has motivated academic researchers to join their industrial colleagues to study atomistic processes of stress generation and relaxation in thin films. The introduction of copper and low dielectric constant materials has given a new urgency to study cracking and debonding in small structures. The fundamental study will impact other major technologies, such as MEMS, integrated photonics, and thermal barrier coatings, where small structure mechanical behavior is important. Vinci and Baker (2002) have edited a multi-author review of the mechanical behavior in small dimensions.

The present method to design reliable small structures, if there is one, rests on continuum mechanics, manifest in handbook solutions, commercial finite element codes, and related measurement protocols. Their inadequacy is increasingly evident when the structures become small, because (among other issues) plastic flows become discrete, and failure phenomena become nucleation, rather than growth, controlled. In the rapidly changing economics of tools for the small, the division of labor has yet been settled: what to understand, what to compute, and

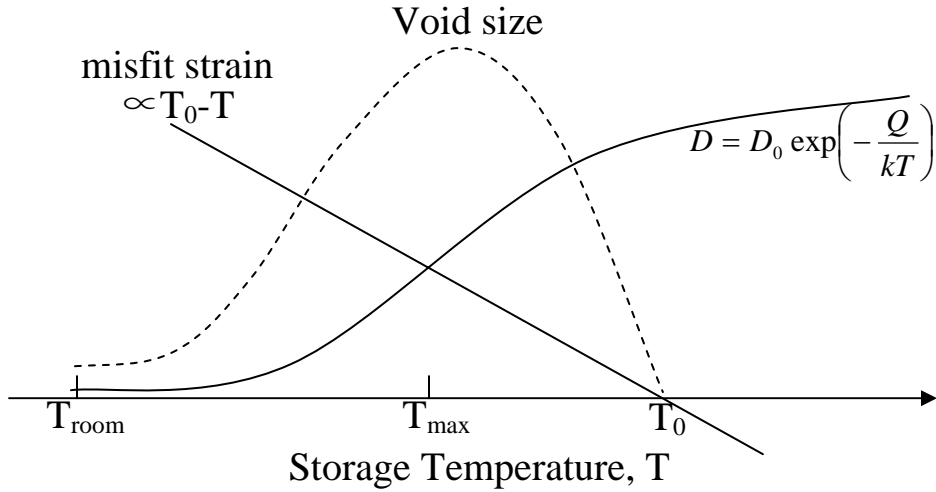
what to measure. And how. The tension between the relentless trend of miniaturization and the disquieting lack of a method to design for reliability will spur innovations for years to come.

Stress-induced voiding (SIV). Early aluminum lines had the width much larger than the thickness. They behaved like blanket films. When narrow aluminum lines were introduced, in early 1980s, with the width comparable to the thickness, voids were observed in such narrow interconnects on wafers held in ovens, or even on wafers left on shelves at room temperature. The voids may sever the interconnects.



Basic understanding. Aluminum has a larger thermal expansion coefficient than silica and silicon. During fabrication, aluminum is encapsulated in silica at a high temperature. On cooling, a narrow aluminum line is in a tensile, triaxial stress state. The magnitude of the stress in aluminum readily exceeds the yield strength of aluminum. Indeed, even a liquid with zero yield strength, so encapsulated, would be under hydrostatic tension. Over a long time, a small piece of a crystal is like a liquid in that they both creep under shear. An encapsulated metal line under uniform hydrostatic tension is in a state of equilibrium: atoms have no motivation to diffuse from one place to another. However, this equilibrium state is metastable. A flaw may act

like a void nucleus. If the stress near the flaw is low or vanishes, the nonuniform stress field motivates aluminum atoms to diffuse away from the flaw, simultaneously growing the void and relaxing the tensile stress. The metal line approaches a stable equilibrium state consisting of voids and unstressed metal.



High temperature storage (HTS) test. This is a commonly used accelerated test. The aluminum line is stress-free at a temperature T_0 , which is close to the silica deposition temperature. Samples are kept in an oven at some temperature T below T_0 . The thermal expansion mismatch volume scales with the temperature drop, $T_0 - T$. It is this mismatch volume that feeds to the void. The atomic diffusivity depends on the temperature as $D = D_0 \exp(-Q/kT)$, where k is Boltzmann's constant, Q the activation energy, and D_0 the pre-factor. As the temperature drops, the mismatch volume increases, but the diffusivity decreases (Figure 39). Consequently, voids grow fastest at a particular temperature T_{\max} . During the storage test, the electrical resistance of a line is measured as a function of time. The line fails if its resistance increases by, say 20%. The time to fail half of the lines, i.e., the median-time-to-failure (MTF), is fit to a semi-empirical relation:

$$\text{MTF} = \frac{C}{(T_0 - T)^N} \exp\left(\frac{Q}{kT}\right),$$

where C and N are fitting parameters, along with T_0 and Q . This relation captures the essence of the above physical considerations. The failure time approaches infinity when the test is carried either at the stress-free temperature T_0 , or at the absolute zero. To obtain the fitting parameters, the storage tests are carried out at several temperatures, possibly around T_{\max} to shorten the testing time. This equation is then extrapolated to predict the failure time at, say, room temperature.

Despite efforts in nearly two decades, there is no single model that accounts for all aspects of SIV. Complicated factors (e.g., grain structures, flaws, interfaces, and atomic transport mechanisms) play roles. Information of such factors is incompletely known, and will probably never be precisely controlled in fabrication. At this point, it seems desirable to consider the physics of the phenomenon semi-quantitatively.

Saturated void volume (SVV). A metal line embedded in a dielectric, such as SiO_2 , is stress-free at some temperature T_0 close to the dielectric deposition temperature, and is cooled to the storage test temperature T . The total number of atoms in the line is constant at all time. Because atomic transport does not change the volume of the metal, the thermal misfit strain is accommodated by a combination of void space and elastic deformation. When the stress in the line completely relaxes, the thermal expansion misfit is fully accommodated by the void space. The saturated void volume (SVV) is

$$V_{sv} = 3\Delta\alpha(T_0 - T)V,$$

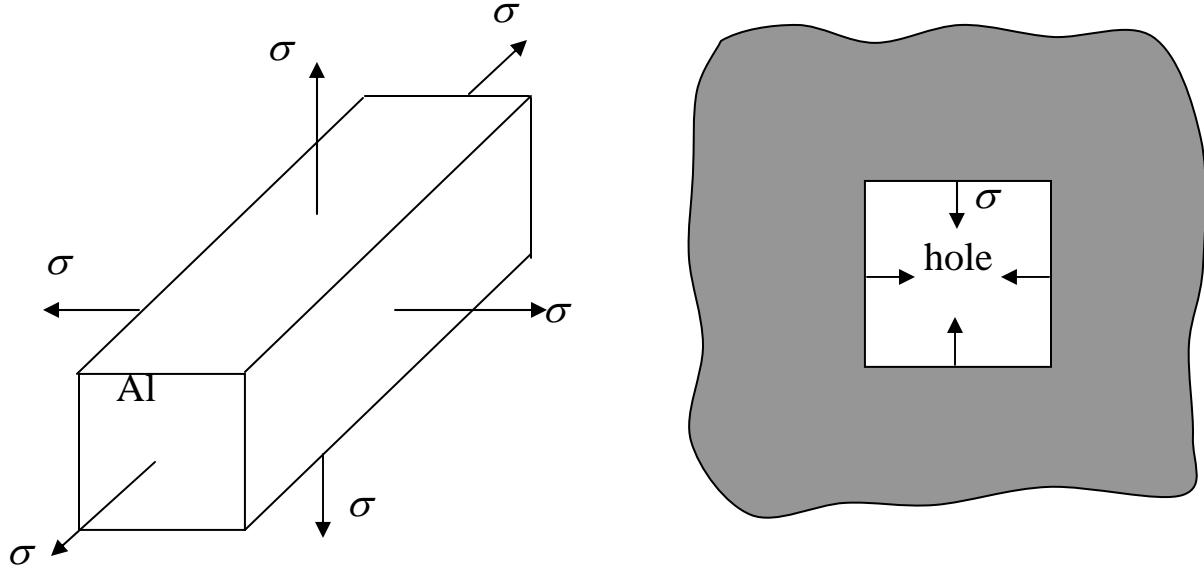
where V is the volume of the metal line, and $\Delta\alpha$ is the effective thermal expansion mismatch strain. If a metal line were embedded in silicon, $\Delta\alpha = \alpha_m - \alpha_{\text{Si}}$, where α_m and α_{Si} are the

thermal expansion coefficient of the metal and silicon. ($\alpha_m = 24 \times 10^{-6} \text{K}^{-1}$ for aluminum and $17 \times 10^{-6} \text{K}^{-1}$ for copper). In an interconnect structure, however, $\Delta\alpha$ depends on all materials in the structure. For the silica-based interconnect structure, because the metals have much larger thermal expansion coefficients than the surrounding materials (silica, silicon, silicon nitride, and tantalum), the thermal expansion mismatch is insensitive to which exact value is used for these other materials; we will use $\Delta\alpha = \alpha_m - 4 \times 10^{-6} \text{K}^{-1}$ in the following estimates. A representative stress-free temperature is 400°C , and a representative storage test temperature is 200°C . Taking these values, one finds that $V_{sv}/V = 1.2\%$ for aluminum, and $V_{sv}/V = 0.78\%$ for copper. For a line of size 1 by 1 by $10 \mu\text{m}$, the saturated void, if it is a single spherical one, has radius 306 nm for aluminum, and 265 nm for copper.

Many voids may nucleate along the metal line, each growing to relax stress in its vicinity. Once the stress completely relaxes, the sum of the volumes of all the voids remains constant as the line is held at the constant temperature. The above equation gives this sum. The actual void volume can be larger or smaller than the SVV. When a line is cooled to a low temperature for a short time, the tensile stress partially relaxes, so that the total void volume is smaller than the SVV. If the line is then brought to a high temperature, for some time the metal is under compression, and the void volume is larger than the SVV. In case of a copper line, we assume that the electroplated copper has been annealed to allow densification prior to encapsulation, so that only thermal expansion mismatch contributes to void volume.

Hydrostatic tension in an encapsulated metal line. The stress field in the metal line is complicated in general, with tensor components and nonuniformity along the line. To grow a large void, atoms must diffuse in the line over a length much larger than the line width. On such a time scale, creep should have relaxed each point in the line to a hydrostatic state. That is, over

a sufficient long time scale, at an elevated temperature, a crystal behaves like a liquid. We will assume that the stress state is hydrostatic in the following development.



The figure illustrates separately the metal line and the dielectric. In the metal line, the stress state has components of an equal magnitude σ in all directions. The stress causes the metal to expand with the volumetric elastic strain σ/B_m , where B_m is the bulk modulus of the metal. When the metal is modeled as an isotropic material, the bulk modulus relates to Young's modulus E_m and Poisson's ratio ν_m as

$$B_m = \frac{E_m}{3(1-2\nu_m)}.$$

For a metal of cubic crystalline symmetry, the bulk modulus relates to its crystalline elastic constants as

$$B_m = (C_{11} + 2C_{12})/3.$$

For aluminum, $C_{11} = 108\text{GPa}$, $C_{12} = 62\text{GPa}$, $C_{44} = 28\text{GPa}$, giving $B_m = 77\text{GPa}$. For Copper, $C_{11} = 168\text{GPa}$, $C_{12} = 121\text{GPa}$, $C_{44} = 75\text{GPa}$, giving $B_m = 136\text{GPa}$. The bulk modulus of copper is about twice that of aluminum.

Regard the encapsulation as an elastic solid with a hole subject to a normal traction of magnitude σ . The dielectric is in a state of plane strain deformation. The traction causes the cross-sectional area of the hole to reduce by $\int u_n ds$, where u_n is the normal component of the elastic displacement at the hole surface. Let A be the cross-sectional area of the hole. Linearity of the elastic field requires that

$$\frac{1}{A} \int u_n ds = -\frac{\sigma}{\mu_{\text{eff}}}.$$

This equation defines an effective modulus μ_{eff} . This effective modulus depends on the shape of the hole, as well as the elastic constants of the dielectric, the barrier, and the silicon substrate (if close by). The effective modulus can be readily calculated using the finite element method. If the cross section is a long rectangle, rather than a square, the system is more compliant, leading to a small μ_{eff} . In the idealized case, when the hole has a circular cross section, and the dielectric is infinite, the stress field in the dielectric is known analytically, and we find that the effective modulus is $\mu_{\text{eff}} = E_d / 2(1 + \nu_d)$, coincident with the shear modulus of the dielectric.

The stress in the metal causes both the metal and the encapsulation to deform. The effective modulus B is given by

$$\frac{1}{B} = \frac{1}{B_m} + \frac{1}{\mu_{\text{eff}}}.$$

If the cross section is a long rectangle, the effective modulus is small, leading to a low hydrostatic stress. In the limiting case when the interconnect is a blanket film, the hydrostatic stress

vanishes in this liquid-like model. For an interconnect of a square cross section, taking $\mu_{\text{eff}} = 30\text{GPa}$ for the silica dielectric, the effective modulus is $B = 22\text{GPa}$ for aluminum/silica structure, and $B = 24\text{GPa}$ for copper/silica structure. Some authors have treated the dielectric as a rigid material, and taken the bulk modulus of the metal, B_m , as the effective modulus. This would significantly overestimate the effective modulus ($B_m / B = 3.5$ for aluminum and $B_m / B = 5.7$ for copper). The mismatch strain is mainly accommodated by the elastic deformation of the dielectric, so that the effective moduli of the two structures are similar, despite the nearly factor two difference in the bulk moduli of aluminum and copper. The effective modulus reduces if the cross section is a long rectangle.

Let θ be the volumetric strain caused, e.g., by the mismatch in thermal expansion coefficients, or densification, or atomic diffusion. This volumetric strain is accommodated by the difference in the volume change of the interconnect line and that of the dielectric hole. Combining the two contributions, one relates the hydrostatic stress in the metal, σ , to the volumetric mismatch strain between the metal and the encapsulation, θ , namely,

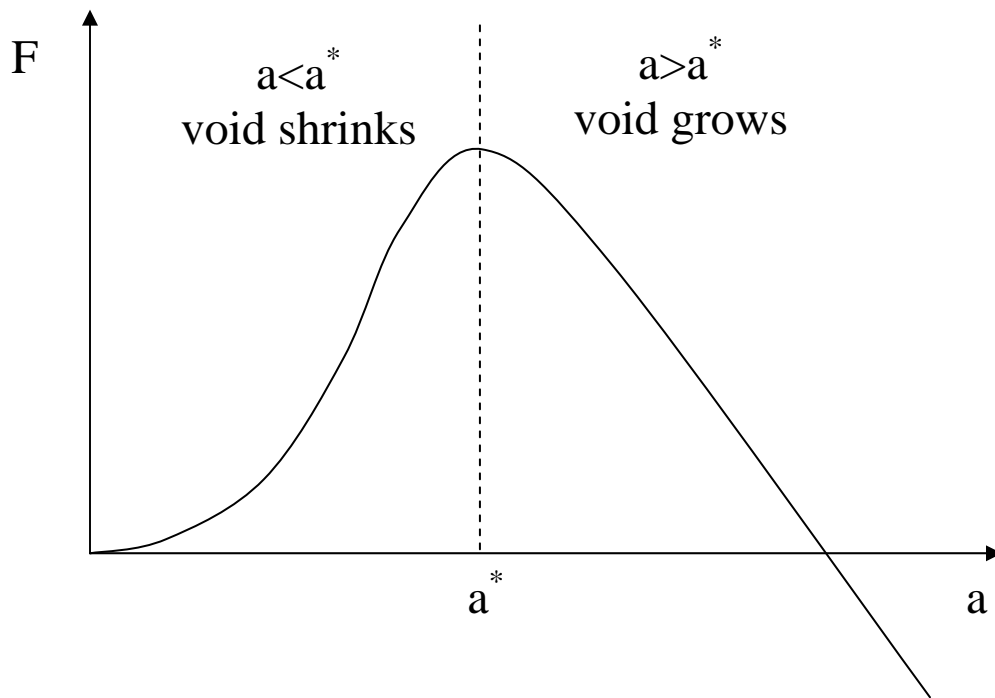
$$\sigma = B\theta.$$

If the volumetric strain θ is entirely due to the thermal expansion mismatch between the metal and the dielectric, for the temperature drop $T_0 - T = 200\text{K}$, the hydrostatic stress is $\sigma = 260\text{MPa}$ in aluminum line, and $\sigma = 187\text{MPa}$ in copper line.

Void initiation. Next consider a small void-like flaw in a metal subject to a hydrostatic stress. The void can change its size by relocating atoms from the void surface into the metal far away from the void. In doing so, the void increases its surface area, and the remote stress does work. The former increases the free energy, but the latter decreases it. Will the void shrink or enlarge? For the time being, we assume that the void volume changes slightly, so that the

number of atoms transported into the line is so small that the stress σ does not change. Take the solid without the void but under the same applied stress as the ground state, at which the system has zero free energy. The current state has a void of radius a . Let γ be the surface energy per unit area. In creating the void, a surface of area $4\pi a^2$ is exposed, raising the free energy of the system by $\gamma 4\pi a^2$. At the same time, atoms occupying the volume $4\pi a^3/3$ relocate, allowing the remote stress to do work $\sigma 4\pi a^3/3$. Thus, the free energy of the system, relative to that of solid with no void, is

$$F(a) = 4\pi a^2 \gamma - \frac{4}{3} \pi a^3 \sigma.$$



When $a = 0$, $F = 0$, which is the ground state. When the void is small, the surface energy dominates, and the void shrinks to reduce the free energy. When the void is large, the stress dominates, and the void enlarges to reduce the free energy. The two behaviors are separated at a critical void radius a^* , at which the free energy maximizes. The critical void radius is given by $a^* = 2\gamma / \sigma$. Taking representative values, $\gamma = 1\text{J/m}^2$ and $\sigma = 200\text{MPa}$, we find that the critical

radius is $a^* = 10\text{nm}$. If the pre-existing flaw size a is known, the flaw can grow if the stress exceeds the value

$$\sigma_{\text{void}} = 2\gamma / a.$$

The above void initiation condition is overly simplistic, and is risky. It assumes an artificial scenario: the metal reaches the hydrostatic state first, and then the flaws start to question themselves whether to enlarge or shrink. In reality, during annealing, the elastic anisotropy between metal grains, as well as the elastic inhomogeneity between the metal and the encapsulation, can momentarily cause very high stresses at various junctions. If atomic transport is slow in relaxing the metal into the hydrostatic state, the high stresses may cause the flaws to grow. Of the two equilibrium states, the hydrostatic state is metastable, but the state with SVV is stable. The voids, once initiated, will grow until the entire line is stress-free.

Stress-driven diffusion. Because the volumetric strain due to thermal expansion mismatch is on the order of 10^{-2} , for a void to grow to a size to sever the line, a long length of the metal has to be relaxed. The long-range diffusion samples averages of various quantities, and is a much more robust process than void initiation. To study mass transport over a length exceeding several times the line width, one can assume that the stress state is hydrostatic, varying along the line and with time. Let the x axis coincide with the line. The stress in the line is a function of position and time, $\sigma(x, t)$. We next formulate a partial differential equation that governs this function.

First consider the *kinematics*. Let J be the atomic flux, i.e., the number of atoms crossing per unit area per unit time. Let θ be the volumetric strain (i.e., the volume loss per unit volume). The flux divergence is accommodated by the strain. Thus,

$$\frac{\partial \theta}{\partial t} = \Omega \frac{\partial J}{\partial x}.$$

Next consider the *energetics*. The nonuniformity of the stress motivates atoms to diffuse to the region of large tension. When an atom is removed from a stress-free solid, and then added to another solid under hydrostatic tension σ , the free energy reduces by $\Omega\sigma$, where Ω is the volume per atom in the metal. For an atom inserted to position, x , the free energy reduces by $\Omega\sigma(x,t)$. For an atom inserted to position $x+dx$, the free energy reduces by $\Omega\sigma(x+dx,t)$. Define the driving force for diffusion, f , as the free energy reduction associated with an atom moving a unit distance. Thus,

$$f = \Omega \frac{\partial \sigma}{\partial x}.$$

Finally consider the *kinetics*. Write Einstein's relation as

$$J = \frac{Df}{\Omega kT}.$$

The diffusivity D is taken to be the average along the aluminum line.

Recall that the mismatch volumetric strain relates to the stress by $\sigma = B\theta$. A combination of the above equations gives

$$\frac{\partial \sigma}{\partial t} = \frac{DB\Omega}{kT} \frac{\partial^2 \sigma}{\partial x^2}.$$

This partial differential equation, together with suitable initial and boundary conditions, governs the evolving pressure distribution, $\sigma(x,t)$.

Lifetime. Assume that the flaw is already large enough so that the stress near the flaw is zero. The above equation is identical to the usual diffusion equation, with the diffusivity-like quantity $DB\Omega/kT$. The solution to this initial-boundary value problem is well known. The time for a void to relax a segment of interconnect of length l scales as

$$t_l \sim \frac{l^2 kT}{DB\Omega},$$

The void fails a line by increasing the resistance of the line to a designated value. Assume that void of length L_1 corresponds to the failure. To grow a void of length L_1 , the segment of the metal line need be relaxed is about $l = L_1 / 3(\alpha_m - \alpha_d)(T_0 - T)$. Inserting into the above equation, we obtain the lifetime

$$t_{\text{life}} \propto \frac{1}{B[(\alpha_m - \alpha_d)(T_0 - T)]^2} \exp\left(\frac{Q}{kT}\right).$$

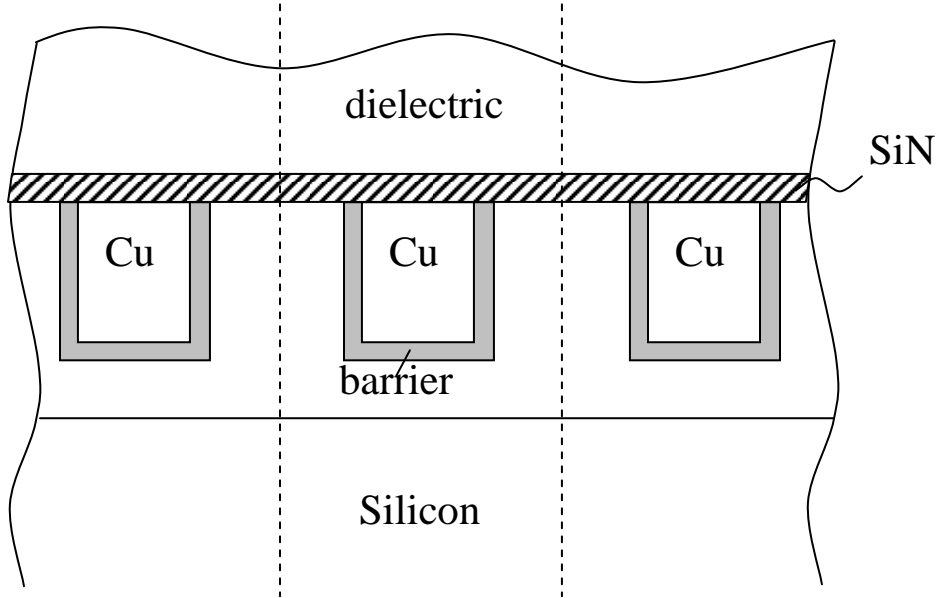
This expression looks similar to the empirical equation given in the beginning of the lecture. As noted before, the effective modulus B depends on the cross section shape, and the dielectric type. Other things being the same, a structure with a smaller B will lead to a longer lifetime.

The effects of low k dielectrics and barriers. A Low k dielectric often has a small elastic modulus and a large thermal expansion coefficient. For example, SiLK has Young's modulus 2.45 GPa and thermal expansion coefficient $66 \times 10^{-6} \text{ K}^{-1}$ (Martin et al., 2000). Will the metal line be under compression on cooling from the fabrication temperature? How small are the effective modulus B and the magnitude of the stress? Does the thin barrier layer between the metal and the dielectric play any role? Because different dielectrics will be used in coming years, it is important to have a convenient method to answer the above questions quantitatively.

The figure illustrates the cross section of several long metal lines embedded in a dielectric. In calculation, one can set the thermal expansion coefficient of every material by its own value minus α_{Si} . Because the Si substrate is bulky, the structure is under a state of plane strain deformation. The adjacent lines provide stiffness to each other. One can take a unit cell containing a single metal line, and prescribe zero displacement on the cell walls. Similar to Fig. 47, remove the metal line from the structure, and leave behind a composite structure of silicon, the dielectric, and the barrier layer. Apply a uniform normal traction σ on the hole surface, and

a temperature change ΔT . The structure is linear elastic, so that the change in the area of the cross section is linear in the temperature change and the applied stress. Write

$$\frac{1}{A} \int u_n ds = 2\alpha_{\text{eff}} \Delta T - \frac{\sigma}{\mu_{\text{eff}}}.$$



The two coefficients α_{eff} and μ_{eff} can be computed by solving the elasticity boundary value problem. The effective thermal expansion mismatch is

$$3\Delta\alpha = 3(\alpha_m - \alpha_{\text{Si}}) - 2\alpha_{\text{eff}}.$$

When the metal has no voids and is under a hydrostatic stress, the stress is given by $\sigma = 3B\Delta\alpha(T_0 - T)$. When the metal grows voids, and the stress in the metal is fully relieved, the SVV is given by $V_{sv} = 3\Delta\alpha(T_0 - T)V$. When the dielectric and the barrier have thermal expansion coefficient similar to silicon, $\alpha_{\text{eff}} = 0$. When the dielectric has a large thermal expansion coefficient, and the barrier is negligibly thin, α_{eff} will dominate. On cooling, the metal is under compression.

The boundary value problem is easily solved by using the finite element method. To appreciate the trend, consider an idealized structure. The metal line has a circular cross section

of radius a , surrounded by a barrier of thickness h_b , which in turn is surrounded by an infinite dielectric. This problem can be solved analytically. The effective modulus μ_{eff} relates to the shear modulus of the dielectric and the barrier:

$$\mu_{\text{eff}} = \mu_d + \mu_b h_b / a ,$$

The effective thermal expansion coefficient is

$$\alpha_{\text{eff}} = \frac{\frac{\mu_d a}{\mu_b h_b} (1 + \nu_d)(\alpha_d - \alpha_{\text{Si}}) + (1 + \nu_b)(\alpha_b - \alpha_{\text{Si}})}{\frac{\mu_d a}{\mu_b h_b} + 1} .$$

When $(\mu_d / \mu_b)(a / h_b) \gg 1$, the dielectric prevails: $\mu_{\text{eff}} = \mu_d$ and $\alpha_{\text{eff}} = (1 + \nu_d)(\alpha_d - \alpha_{\text{Si}})$. When $(\mu_d / \mu_b)(a / h_b) \ll 1$, the barrier prevails: $\mu_{\text{eff}} = \mu_b h_b / a$ and $\alpha_{\text{eff}} = (1 + \nu_b)(\alpha_b - \alpha_{\text{Si}})$. A representative set of magnitudes are $\mu_d / \mu_b = 0.01$, $a / h_b = 10$, $(\mu_d / \mu_b)(a / h_b) = 0.1$. When the barrier prevails, the saturation void volume is comparable to that in copper/silica structure. Taking $\mu_b = 60\text{GPa}$ and $a / h_b = 10$, we obtain that $\mu_{\text{eff}} = 6.0\text{GPa}$. For copper interconnect, the barrier provides the effective modulus $B = 5.7\text{GPa}$. Even with a dielectric of negligible stiffness, the barrier itself can provide significant constraint.