EM 388F

Fracture Mechanics

Term Paper

Channel Cracking in Low-K Interconnect Structures

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Abstract[1~7]:

Continuous scaling of high-performance Ultra Large Scale Integrated (ULSI) circuits requires the integration of low dielectric constant (low-κ) materials for interconnect structures. However, low k material is mechanically weak and has low fracture toughness，which may result in film cracking during fabrication of the back-end-of-line (BEOL), delamination during packaging.

One of the major failure mechanism observed for low k films during the wafer manufacturing process is channel cracking, in which the cracks propagate in the film plane. When multilayer structures like cu/low k interconnects are manufactured, a large thermal stress will be generated in the film because of the stiffness and CTE difference between Si substrate and low k materials, which may lead to channel cracking in the low k films. In this study, the mechanics of channel cracking will be analyzed and analytical solution is deduced following Z. G. Suo's method[5,9]. Experimental measurement of the film toughness is also covered. A finite element model used to simulate the channel cracking in low k films is discussed. Effect of multilayer structure configuration such as buffer layer, Cu pad gap width and film thickness on channel cracking is investigated.

Introduction[1~7]:

As the semiconductor industry strives to increase the electrical performance of their chips, insulator film with a lower dielectric constant (k) is required to reduce the RC delay and cross talk between lines. The introduction of copper and low dielectric-constant materials in the interconnect layers presents a significant challenge to the development of reliable package assembly processes and give a new urgency to study cracking and debonding in small structures for low k dielectrics. This is mainly due to the weak mechanical properties of the low k film compared to those of silicon dioxide previously used. For example, the properties of organosilicate materials are about five times weaker than those of silicon dioxide. The reduced mechanical properties can result in channel cracking in the film during the BEOL fabrication, delamination during assembly and other reliability concerns.

Industry has been working on several different low k materials to replace silicon dioxide, such as organosilicate glass (OSG) which is also known as carbon-doped oxides (CDO), carbon-doped silicate (CDS) and PECVD SiCOH film. However, the development and implementation of these low k films are not as easy as anticipated. Various reliability problems were observed during the BEOL fabrication and packaging process, in which channel cracking is a major failure mode especially when multilayer interconnect structures were build. A typical multilayer Cu/low k interconnect structure for 90nm technology node is shown in Figure 1. Seven metal layers were built into the structures with low dielectric films in between. Figure 2 gives an example of the channel cracking failure in the low k films during manufacturing. [1]

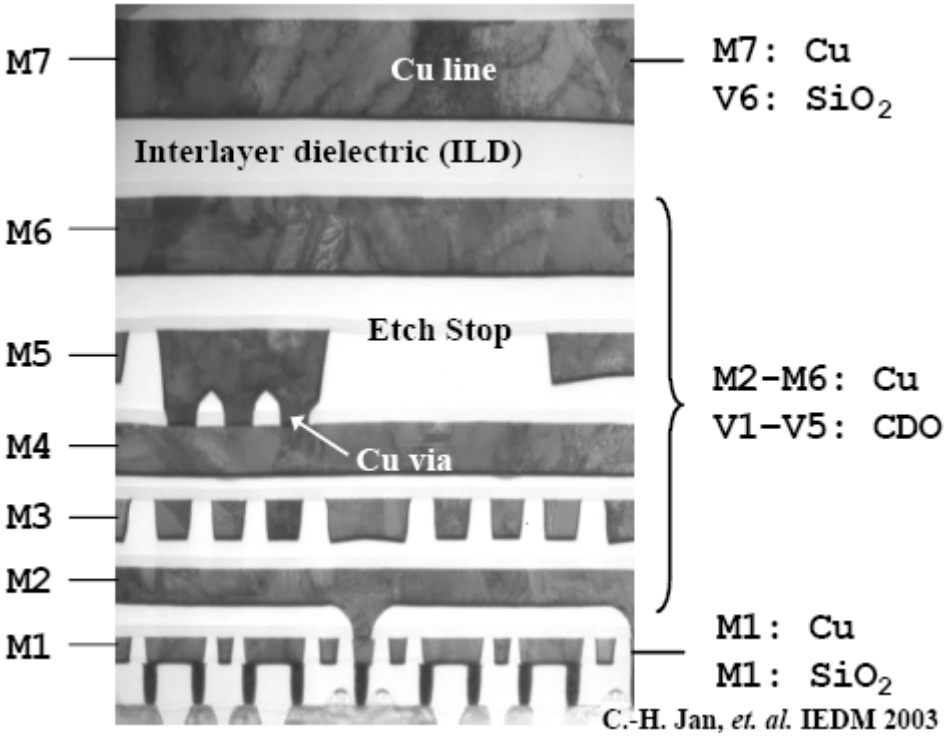

Figure 1: Cu/low k interconnect for 90nm technology node [1]

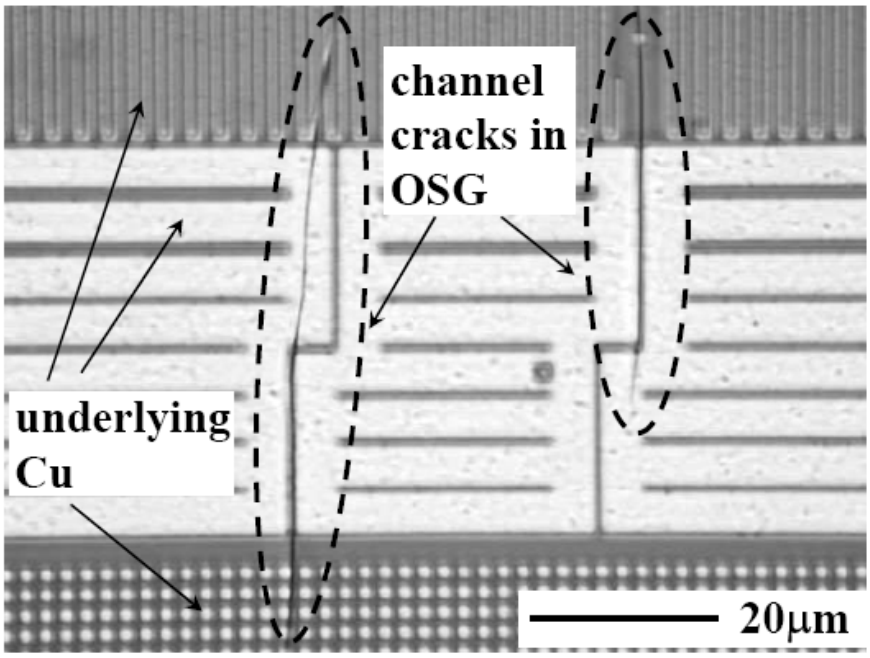

Figure 2: Channeling cracks inside OSG film during BEOL fabrication [1]

Mechanics of film channel cracking[1,2,3,5,9]:

Figure 3 shows a crack channeling through a film. In the steady state, the energy release rate at the channel front can be evaluated using two plan problems by subtracting the strain energy stored in unit slice far behind of the front from that far ahead.

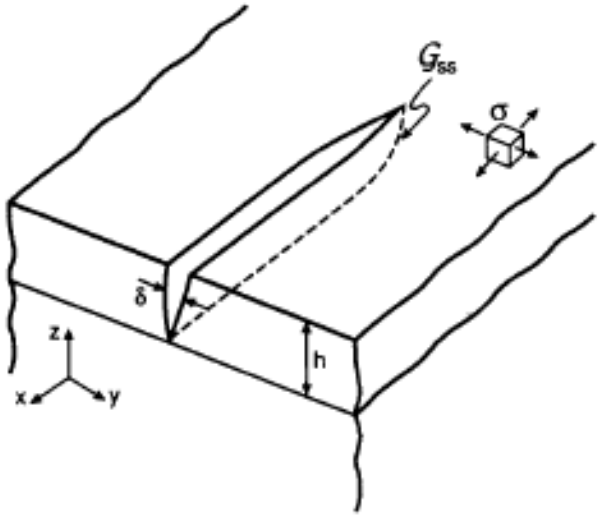

Figure 3 A channeling crack in a film driven by tension [9]

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Two formulae have been developed according to this theory. One is

$$G_{ss} = \frac{1}{2h}\int_0^h \delta(z)\sigma(z)\,dz.$$

$\sigma(z)$ represents the stress distribution on the crack plane before cracking.

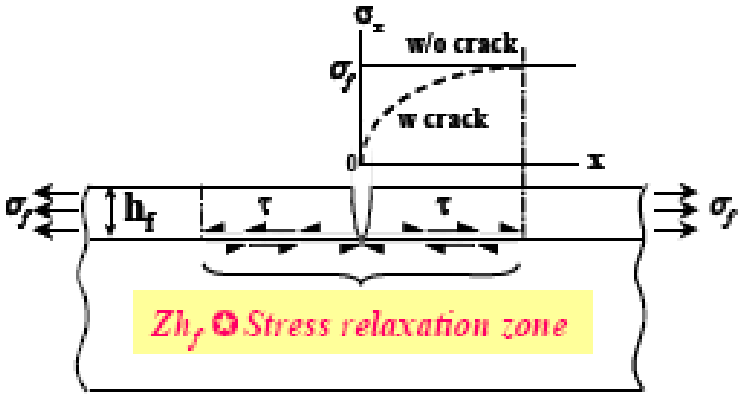
$\delta(z)$ represents displacement profile for a plane strain crack

The second formula is

$$G_{ss} = \frac{1}{h}\int_0^h G(a)\,da,$$

Where G(a) is the energy release rate of a plane strain crack of depth a. Both formulae are valid for films and substrates with dissimilar elastic moduli.

For the first formula, when the crack length a is much larger than the film thickness h, the stress field in the crack becomes invariant as the crack propagates. The volume in which the stress relaxes scales as ah^2 [1]



So the total elastic energy change is

$$\Delta U \sim \frac{ah^2\sigma^2}{E_f}$$

The energy release rate is

$$G = \frac{\Delta U}{\Delta A} = Z\frac{ah^2\sigma^2}{E_f ah} = Z\frac{h\ \sigma^2}{E_f} \qquad (1)$$

Where $h,\ \sigma,$ and $\bar{E} = E/(1-\nu^2)$ represent the film thickness, film residual thermal stress, and plane-strain elastic modulus, respectively. The dimensionless number Z depends on the elastic constants of the film and the substrate. The number must be determined by solving the boundary value problem and can be expressed as a function of plane-strain Dundurs parameters:

$$\alpha = \frac{\bar{E}_f - \bar{E}_s}{\bar{E}_f + \bar{E}_s}, \qquad \beta = \frac{\mu_f(1-2\nu_s) - \mu_s(1-2\nu_f)}{2\mu_f(1-\nu_s) + 2\mu_s(1-\nu_f)},$$

In which u and v represent shear modulus and Poisson's ratio. Figure 4 gives the Z value as a function of elastic mismatch between film and substrate.[3]

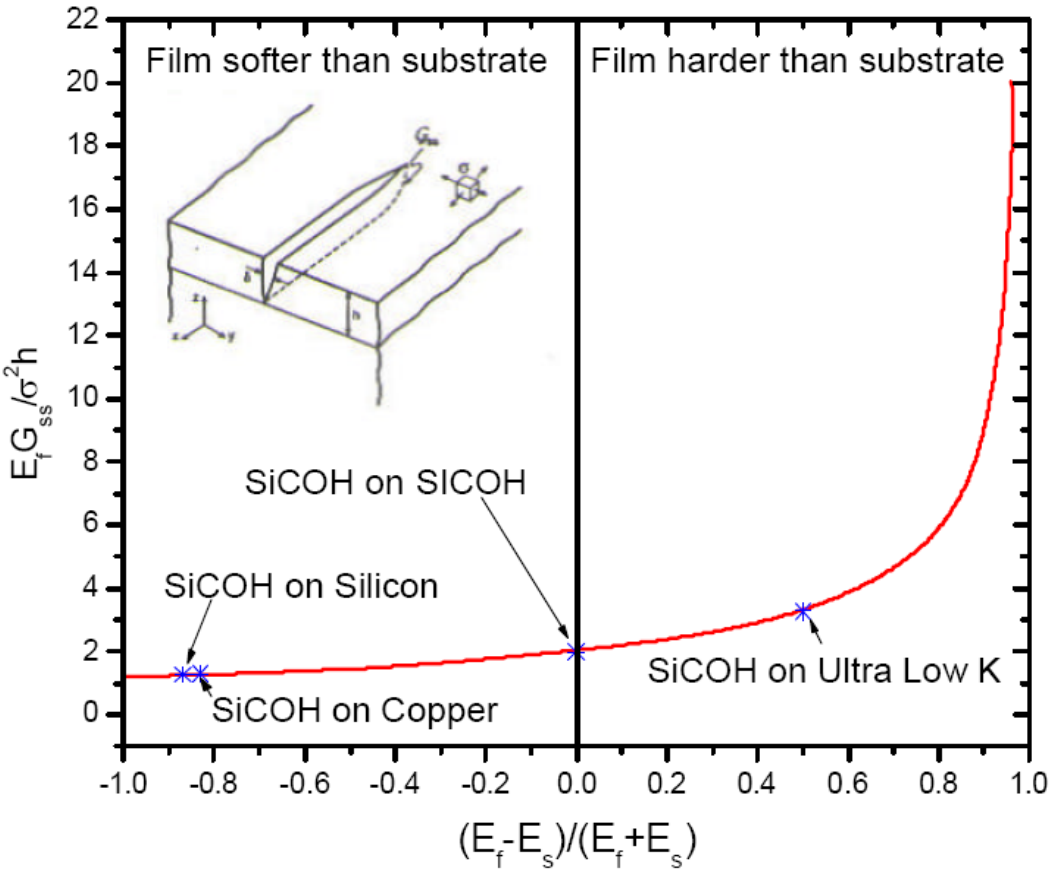


Figure 4: Dependence of Z on elastic mismatch between the film and the substrate[3]

As shown in the curve, when the thin film and substrate have similar elastic constants, Z=2.0, When the substrate is stiffer than the film, Z is between 1 and 2 and does not vary significantly. When the substrate is much more compliant than the film, Z can be very large. [3]

Z also depends on the properties of the underlying layer underneath the low k film. Compliant underlying layer enhances Z. For example, figure 5 shows a channeling crack in low k film with SiLK underlying layer, the dependence of Z on the thickness of SiLK layer is plotted in figure 6.

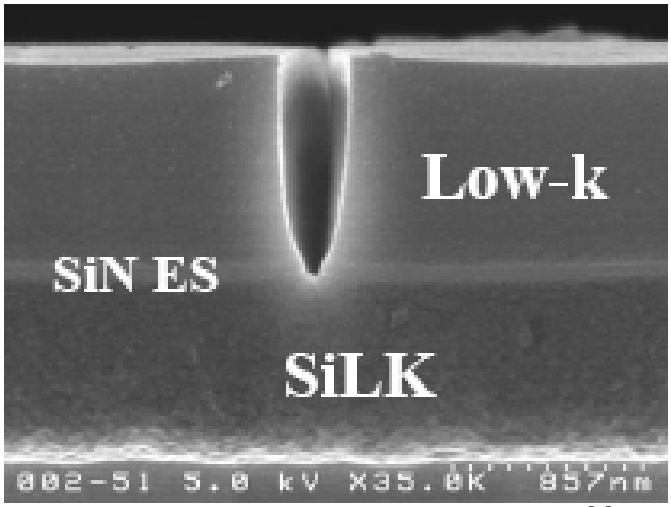


Figure 5 Schematics of the test structure [2]

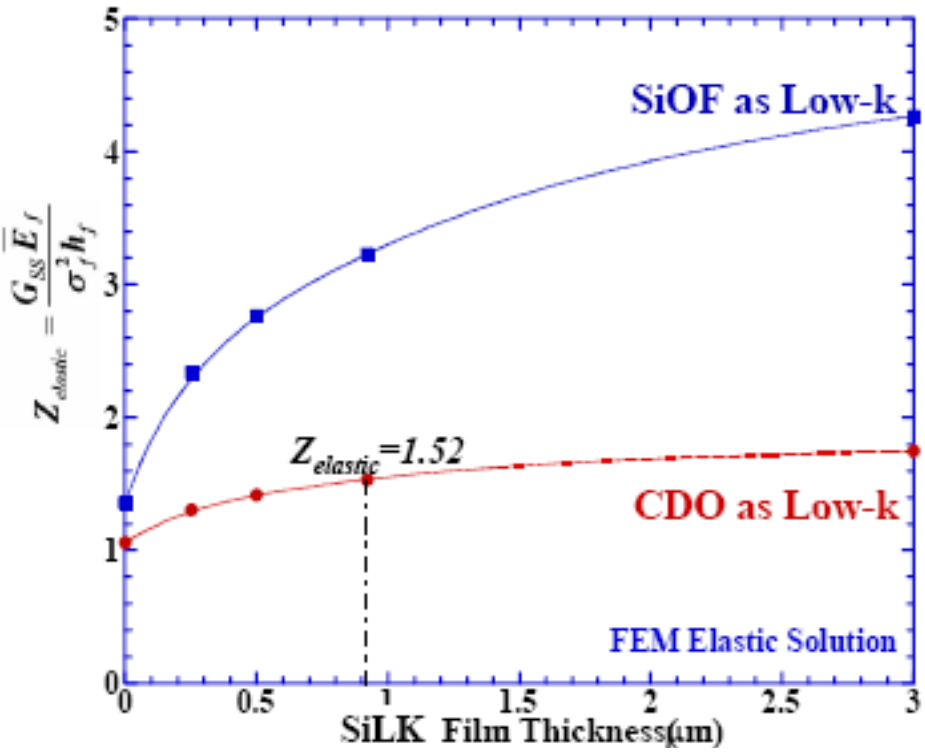


Figure 6 Effect on underlying layer [2]

The result demonstrated that for both SiOF and CDO film Z increases as the underlying SiLK film gets thicker and finally reaches saturation. The mechanical properties of underlying layer also have significant impacts on the energy release rate of channeling crack. [2]

Thin film toughness measurement[1,9,10]:

Ma et al. [10] have developed a technique to measure thin film toughness. The test procedure consists of two steps: (a) Generating pre-cracks, a convenient way of generating precracks is by scratching the surface using a sharp object. Care must be taken to generate cracks just in the film, but not in the substrate. (b) Propagating the

cracks using controlled stress. Use a bending fixture as shown in figure 7 to load the sample, and a digital camera to record the crack growth events. After a crack propagates some distance away from the scratch, the crack grows at a steady velocity. By recording crack growth at slightly different bending loads, one can measure the crack velocity as a function of the stress. The steady velocity is very sensitive to the applied stress. Consequently, the critical stress is accurately measured by controlling the velocity within a certain range that is convenient for the experiment. The critical energy release rate can be obtained by

$$G == Z\frac{h\ \sigma_{critical}^{\ 2}}{E_f}$$

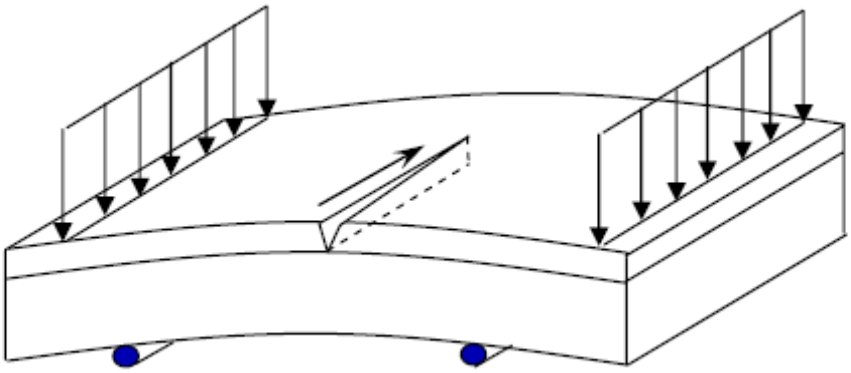


Figure 7 Bending test for channel crack measurement [1]

The measured velocity of isolated cracks as a function a energy release rate was given in Figure 8, linear relationship was obtained. [1]

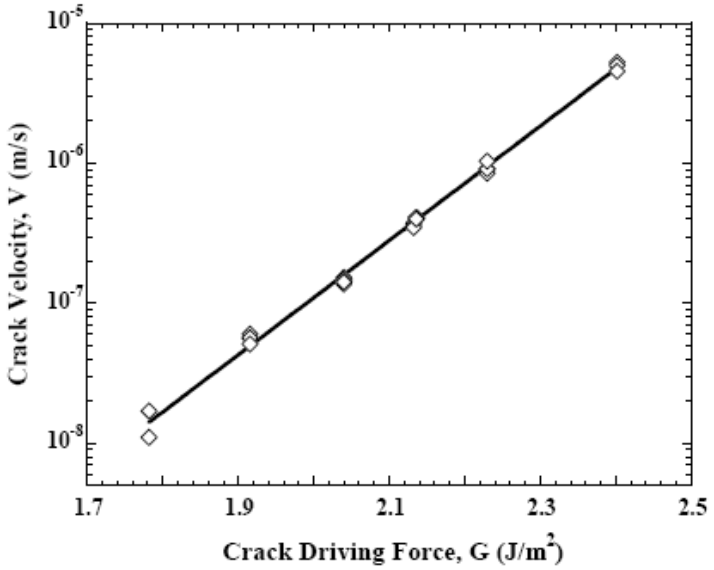


Figure 8 V-G plot [1]

Constrain effect on channel cracking in low k thin films[2,3]:

Effect of underlying layer on crack propagation in carbon-doped silicate films was studied by Ting Tsui, etc.[2]. CDS films were deposited using plasma-enhanced chemical vapor deposition (PECVD) near 400C. Thin films with elastic moduli greater and smaller than CDS were used as underlying layer between the Si substrate and the CDS film. In his study, both SiNx and SiO2 materials were used. Both materials have modulus greater than CDS, but smaller than silicon substrate. The configuration is shown in figure 9. Crack velocity for a 3.25um CDS film is plotted as a function of the thickness of SiNx and SiO2 layer in figure 10.

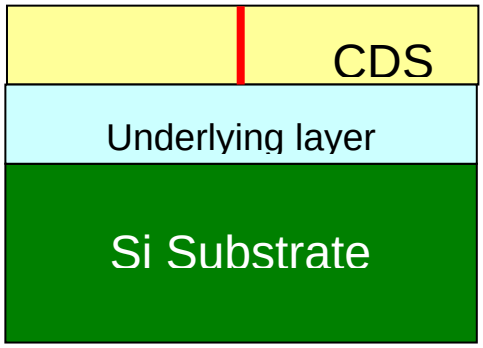
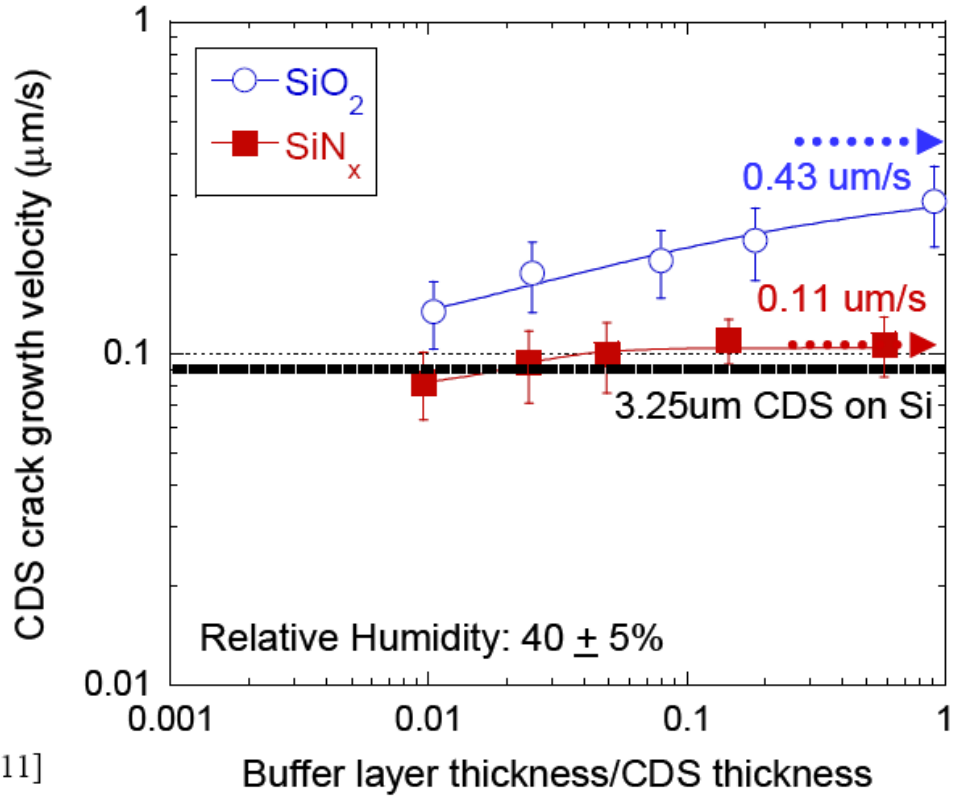


Figure 9 Schematics of test structure



:s [11]

Figure 10 Effect of buffer layer thickness [2]

The channel crack velocity for a CDS film of the same thickness deposited on bare silicon is used as a reference. The result shows that channel cracks grow faster on buffer layers than on Si. The material properties, residual stress, and thickness of the CDS film do not depend on the buffer layer. According to Eq. (1), the increased crack growth velocity must be attributed to the greater energy release rate applied to the CDS film as a result of the SiN_x and SiO_2 buffer layers. [2]

Since the SiN_x and SiO_2 buffer layers are more compliant than the substrate, the constraint on the cracked film is reduced and this causes the value of *Z* to increase, which causes larger energy release rate and crack propagation velocity as shown in Fig. 10. The comparison between the SiN_x and SiO_2 buffer layers also confirmed the conclusion. CDS films with a SiO_2 buffer layer have greater crack velocities than those with a SiN_x layer because SiO_2 (E~70Gpa) is more compliant than SiN_x (E~155Gpa). Another import result from their experiment is that as the buffer layer thickness increases, the channel crack velocity approaches a steady state. These limits correspond to the velocity of a channel crack in a CDS film deposited on a substrate made of buffer layer material and are marked by the arrows in Fig. 10 [2].

The crack propagation rate results discussed above demonstrated that a compliant buffer layer can significantly alter the cracking behavior by reducing elastic constraint from the silicon substrate. Since Cu/low k interconnects are usually multi-layer structures, T. Tsui etc.[2] also investigated how BEOL multi-layer structures that consist of alternating layers of a low-k dielectric and a stiff etch-stop material affect the elastic constraint and crack growth rate. In this study, samples were prepared by depositing one to ten bi-layers comprised of a 300 nm low-k dielectric and a 60 nm silicon carbo-nitride (SiCN) etch-stop. Three different bi-layer systems with different low-k materials were tested representing three generations of BEOL technology nodes – SiO_2 (130 nm node), CDS (90 nm), and LD-CDO (45 nm and beyond). All bi-layer samples were capped with 3 μm thick CDS films. The CDS channel crack propagation rates are plotted in Fig. 11 as a function of the number of bi-layers deposited beneath the CDS films. The figure shows that crack velocities for the three dielectric systems increase as the number of bi-layers increases and approach to a steady state finally. A reduction in elastic constraint is indeed expected as all of the bi-layer materials have smaller elastic modulus values than the silicon substrate. It is important to note that, at the tenth bi-layer, the crack propagation rate in the LD-CDO/SiCN system (45 nm node) is approximately five orders of magnitude faster than that in SiO_2/SiCN (130 nm node), indicating that channel cracking will be a significant challenge for the future 45 nm technology node and beyond.

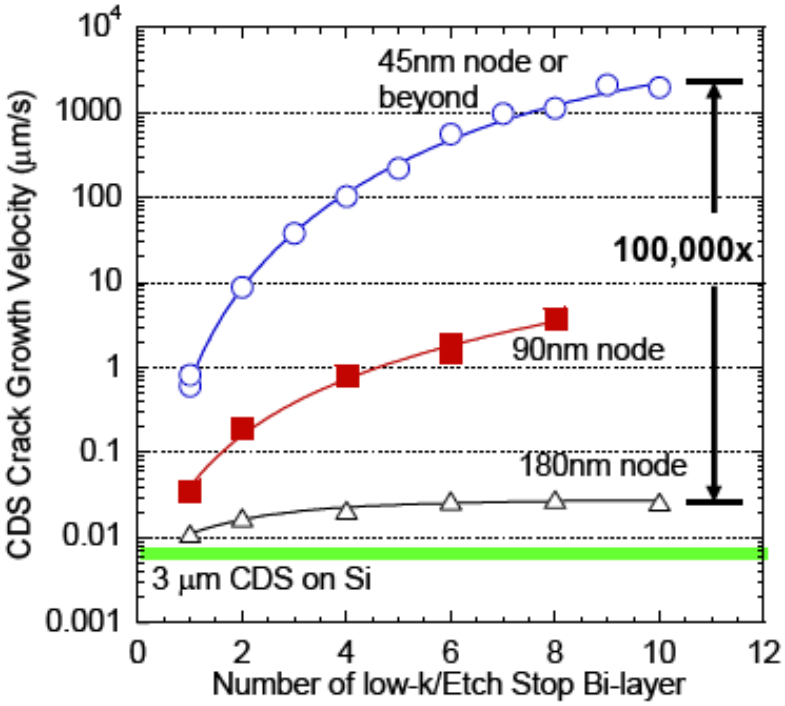


Figure 11 CDS crack growth velocity as a function of low k layers [2]

Effects of multilayer structure configuration on channel cracking[1,3,4,7]

As shown in figure 1, in the Cu/low k interconnects, low k films was usually deposited on top of patterned film instead of blank film. As the feature size keeps scaling down as technology advances, the gap between metal pads is getting smaller. The effect of the gap width on energy release rate of channeling crack is investigated by X.H. Liu [3] using a structure as shown in figure 12. Dimensional analysis indicates that the ERR has the following functional form

$$G/G_o = F(x/h_c, w/h_c, h_u/h_c, h/h_c)$$

In this equation, it is clearly stated that the ERR will depend on the geometry of multilayer structures. Considering a channeling crack at the center of the gap w, which has the maximum driving force, X.H. Liu [3] and J. He[1] calculated the crack energy release rate for different gap width, underlying layer thickness, etc. to study the effect of pattern of multilayer structure. The CDO film on blanket film is used as a reference.

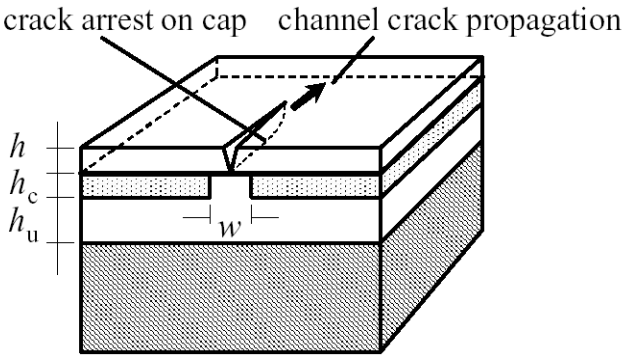


Figure 12 ERR Calculation model [3]

As shown in figure 13, the energy release rate increases as gap width reduces, reaching maximum when w is about 3 times of copper thickness, then decreases quickly. The peak G is about 2 times of $G_{blanket}$, indicating the copper layer greatly enhances the driving force due to the thermal mismatch and stiffness differences between Cu and low k materials. And the peak portion of the curve should be avoided for the pattern design.

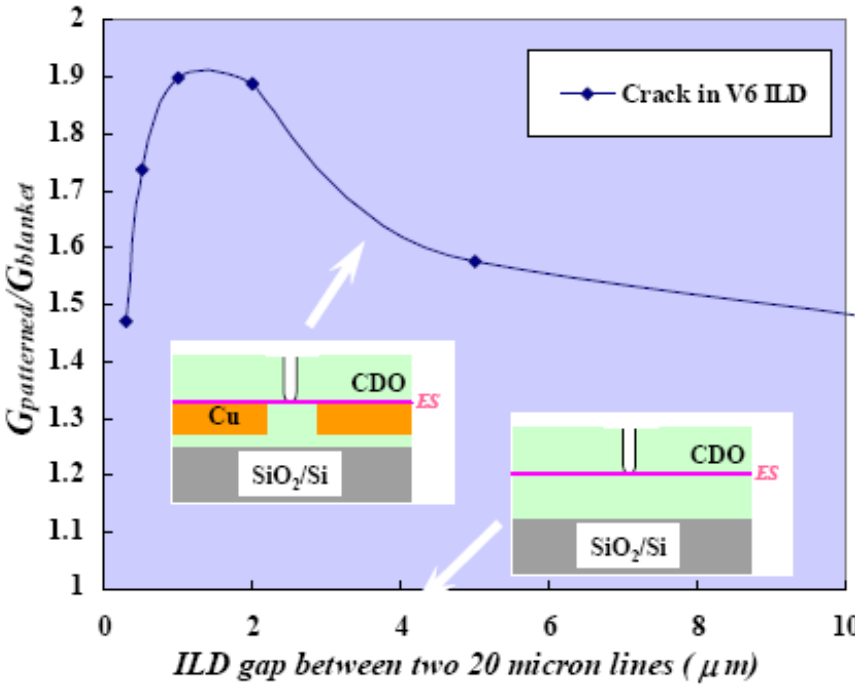


Figure 13 Gap width effect on the ERR [1]

The underlying layer thickness also has impact on the channel cracking behavior according to X.H. Liu[3] as shown in figure 14. Two different gap widths were considered for thickness effect. The figure shows the ERR increases with thickness of underlayer low k film thickness.

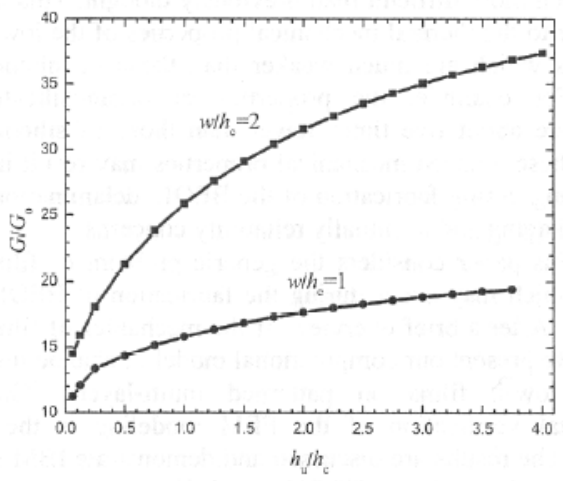


Figure 14 underlayer thickness effect on ERR [3]

Summary [1~11]:

The energy release rate of channeling crack depends on the film thickness, mechanical properties and also the constraints on the film. It has been demonstrated by J. He and T. Tsui, etc., that the elastic properties and thickness of underlying layers have a huge impact on the channel cracking behavior. The energy release rate is reduced if the underlying layer is more compliant than the substrate. The constrain effect of underlying layer increases with the thickness. And when the underlying layer grows to multi-layer structures, the energy release rate of top film will be further increased, posing great challenges for future technology nodes.

From the simulation results by X. H. Liu, we know that the geometry of multi-layer thin films has a great effect on the crack energy release rate too. By optimizing the structure and the thin film properties, we can decrease the crack driving force, thus preventing the multilayer interconnect structure from failure. These observations have important implications for the reliability of weak low k films.

References

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